NM25LQ512A Datasheet

1.8V 512Mbit Serial Flash Memory with Standard/Dual/Quad SPI DPI and QPI

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  - Totally 65536K bytes
  - 256-byte Page Program
  - 4KB Subsector/32KB Subsector/64KB Sector/Bulk Erase
- **Protocols Supported**
  - SPI :
    - ◆ Standard : SCLK, CS#, SI, SO, WP#, HOLD#
    - ◆ Dual : SCLK, CS#, IO0, IO1, WP#, HOLD#
    - ◆ Quad : SCLK, CS#, IO0, IO1, IO2, IO3
  - DPI : SCLK, CS#, IO0, IO1, WP#, HOLD#
  - QPI : SCLK, CS#, IO0, IO1, IO2, IO3
  - SPI/DPI/QPI: DTR Read Mode
- **Single Supply Voltage**
  - Full voltage range: 1.7~2.0V
- **High Performance**
  - 120MHz maximum clock frequency
  - Dual data throughput up to 240Mbit/s
  - Quad data throughput up to 480Mbit/s
  - DTR quad data throughput up to 720Mbit/s
  - Page Program: 0.45ms typical
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  - UT: From -40℃ to +125℃
- Endurance of 100,000 Program/Erase Cycles
- Data Retention of 20 Years
- Industry Standard Packaging
  - SOP8, SOP16
  - DIP8
  - WSON8
  - TFBGA-24

2. General Description

The NM25LQ512A is a 512Mbit Serial Peripheral Interface (SPI) NOR Flash memory device which supports standard SPI interface with Dual/Quad capabilities, DPI mode, QPI mode and DTR read modes.

The main array of the device can be viewed as a 64M-byte array of data bytes, which can be erased at a variety of granularities, programmed in 256-byte pages and read for any number of bytes. Its chip pins include: SCLK, CS#, SI (IO0), SO (IO1), WP# (IO2), HOLD# (IO3) and RESET#.

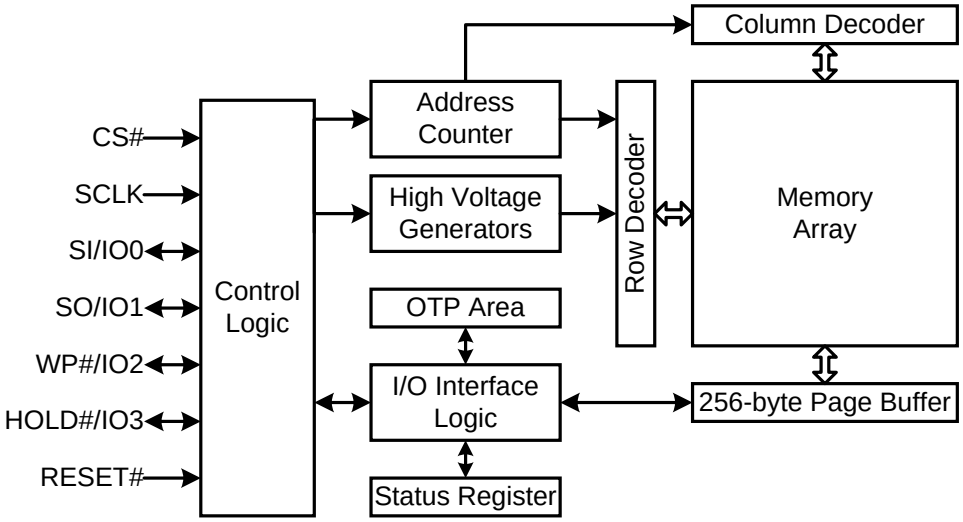
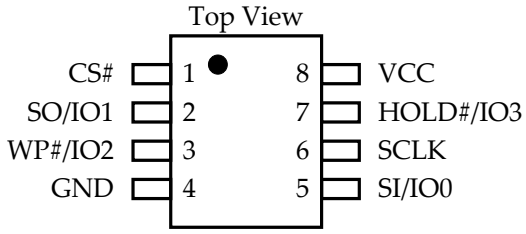


Figure 1: **NM25LQ512A SPI Flash Block Diagram**

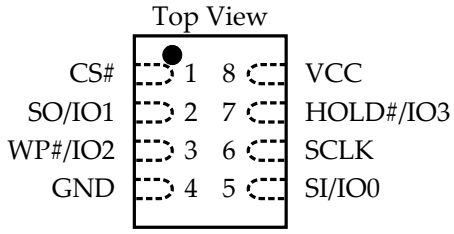
3. Pin Configuration

The NM25LQ512A device has the following pin configurations.

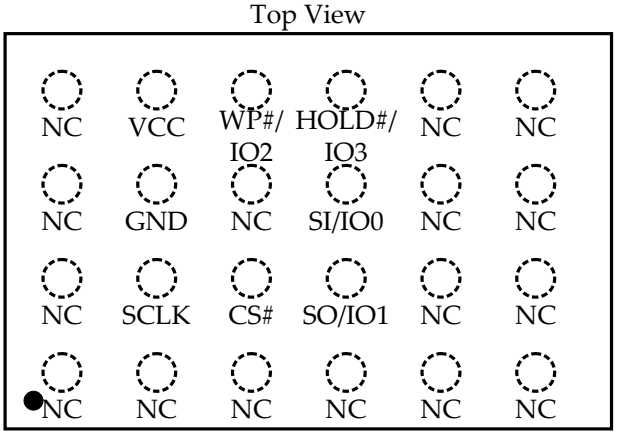
8-PIN SOP, 8-PIN DIP



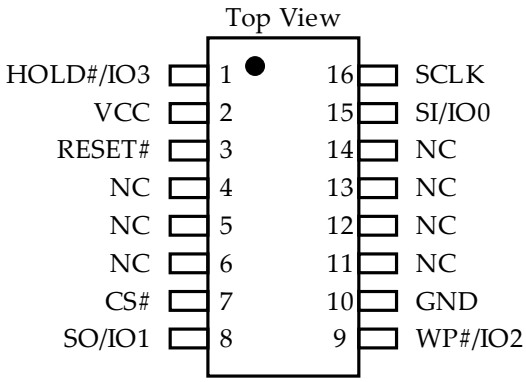
8-PIN WSON, 8-PIN USON



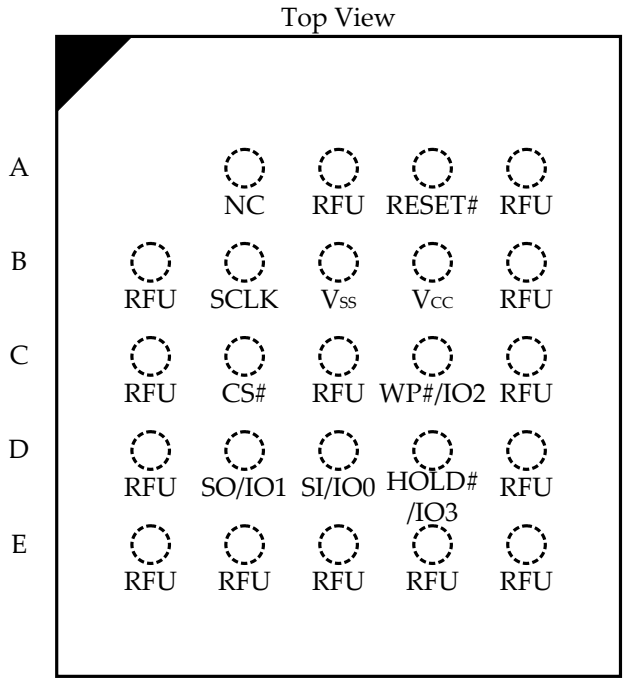
24-PIN TFBGA



16-PIN SOP



24-PIN T-PBGA



27-Ball XFWLBGA

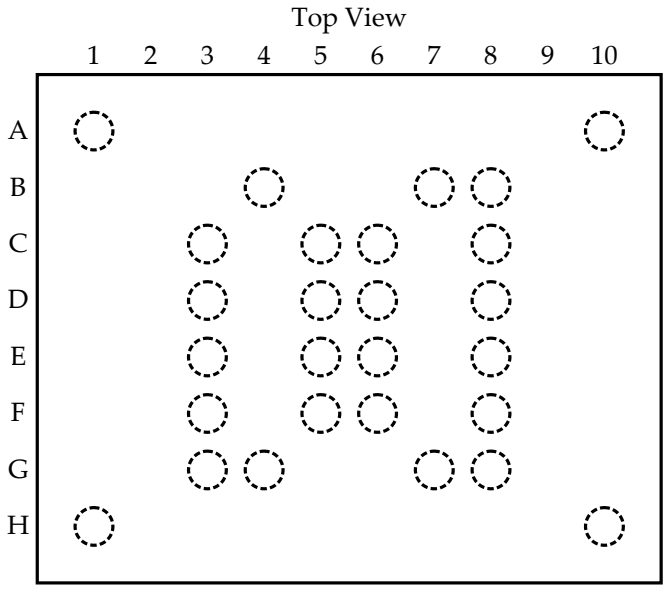


Figure 2: **Pin Map**

4. Pin Description

The NM25LQ512A SPI Flash memory device operates with a single power supply of 1.8V typical.

Table 1: **Pin Definitions**

Signal	Direction	Description
CS#	Input	Chip Select, active low
SCLK	Input	Clock Input
SI/IO0	Input/Output	Serial Data Input in standard SPI; IO0 in Dual SPI, Quad SPI, DPI and QPI.
SO/IO1	Input/Output	Serial Data Output in standard SPI; IO1 in Dual SPI, Quad SPI, DPI and QPI.
WP#/IO2	Input/Output	Active low Write Protect in standard SPI; IO2 in Quad SPI and QPI.
HOLD#/IO3	Input/Output	Active low Hold Input in standard SPI; IO3 in Quad SPI and QPI.
RESET#	Input	Active low reset input that resets the device.
V_{CC}	-	Power Supply
GND	-	GND

4.1. Chip Select (CS#)

The Chip Select (CS#) pin enables and disables device operations.

When CS# is high, the device is deselected and all data output pins are at high impedance state; the device is in standby mode with standby level of power consumption if Write Status Register, program or erase operations are absent.

When CS# is low, the device is selected, available for incoming commands.

4.2. Clock Input (SCLK)

The clock input provides a reference of the synchronization of the SPI interface.
For STR commands, all inputs are latched on the rising edge of SCLK, while all data shifts out on its falling edge. For DTR commands, inputs are latched on both rising and falling edges of SCLK, and data shifts out on both edges as well.

4.3. Serial Input (SI/IO0)

Serial input is a unidirectional pin in Standard SPI mode, which is the input for all commands, address and data. In Dual SPI, Quad SPI, DPI and QPI modes, SI functions as an bidirectional IO0, which transfers command, address and data information.

4.4. Serial Output (SO/IO1)

SO is unidirectional in Standard SPI mode for the output of all internal status and data. In Dual SPI, Quad SPI, DPI and QPI modes, SO functions as an bidirectional IO1, which transfers command, address and data information.

4.5. Write Protect (WP#/IO2)

The WP# Write Protect function is available only if device not in extend-SPI protocol with QOFR or QIOFR, or QIO-SPI protocol. The WP# pin in conjunction with SRP0 bit protect the Status Register from unwanted modifications.
During the extended-SPI protocol with QOFR and QIOFR in-structure, and with QIO-SPI protocol, the WP# function is disabled and this pin functions as a dedicated IO2 data pin, which transfers command, address and data information.

4.6. HOLD (HOLD#/IO3)

The HOLD# function is available only if reset/hold bit of nonvolatile or enhanced volatile configuration register are work. Driving the HOLD# pin low halts all serial communications of the device, without affecting any ongoing Write, Program or Erase operations in progress. During hold state, all outputs are released to high impedance, and SI and SCLK are ignored by the device. Deasserting CS# while HOLD# is low will reset the internal logic of the device.
SCLK and HOLD# controls the entrance and exit of hold state. A falling edge of HOLD# during SCLK=0, or falling edge of SCLK during HOLD#=0 brings the device into HOLD state; a rising edge of HOLD# while SCLK=0, or falling edge of SCLK while HOLD#=1 brings the device out of HOLD state. The CS# should keep low during HOLD state.

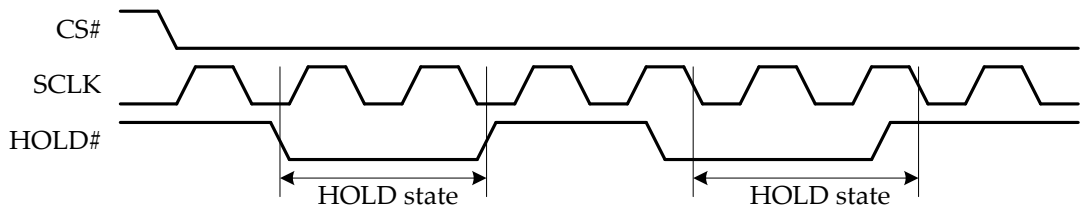


Figure 3: **HOLD Condition**

When the device is in Quad SPI or QPI mode, the HOLD# function is disabled and this pin functions as dedicated IO3 data pin, which transfers command, address and data information.

4.7. Reset Input (RESET#)

During reset, all outputs of the device are tristated. Attempting to reset the device during Write, Program or

Erase operations may result in data loss. After reset, the device returns to standby mode, and all volatile bits return to the default value.

5. Interface Protocols

5.1. Standard SPI

The NM25LQ512A device supports standard SPI with a four-signal bus: CS#, SCLK, SI and SO. Both mode 0 and mode 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

In standard SPI mode, a command is communicated solely via SI pin and spans 8 SCLK cycles regardless of DTR mode setting.

5.1.1. Dual SPI

The device features a number of Dual SPI operations; during these commands, SI and SO pins become IO0 and IO1. Data is transferred using IO0 and IO1, doubling the throughput of Standard SPI mode.

5.1.2. Quad SPI

The device also features a number of Quad SPI operations; during these commands, SI, SO, WP# and HOLD# become IO0, IO1, IO2 and IO3, respectively. Data is transferred using IO0 through IO3, offering four times the throughput of Standard SPI mode.

If Quad SPI is activated, it is strictly forbidden to tie WP# and HOLD# to power supply or GND to prevent signal conflict which may damage the device permanently.

5.2. Dual Peripheral Interface (DPI)

The device supports Dual Peripheral Interface (DPI) operation mode which employs IO0 and IO1 pins to communicate command, address and data information. DPI mode is enabled or disabled by the DPIB configuration bit.

In DPI mode, a command is communicated via IO0 and IO1 pins and spans 4 SCLK cycles regardless of DTR mode setting.

5.3. Quad Peripheral Interface (QPI)

The device also features Quad Peripheral Interface (QPI) operation mode which employs all four IO (IO0, IO1, IO2, IO3) pins to communicate command, address and data information. QPI mode is enabled or disabled by the QPIB configuration bit.

In QPI mode, a command is communicated via IO0, IO1, IO2 and IO3 pins and spans 2 SCLK cycles regardless of DTR mode setting.

5.4. Single Transfer Rate (STR) and Double Transfer Rate (DTR)

The NM25LQ512A device features both Single Transfer Rate (STR) and Double Transfer Rate (DTR) modes.

In STR mode, the device samples input signal on SCLK rising edge and shifts out data on SCLK falling edge, while DTR mode enables address and data to be latched into and out of the device on both rising and falling edges of SCLK clock signal. DTR mode can further increase data throughput of the device.

6. Device Organization

The NM25LQ512A utilizes a variety of registers and memory array to store control information and user data.

6.1. Identification

The NM25LQ512A device has IDs and a unique ID that can be accessed by the user.

The unique ID is 17 bytes long; it is unique to each device and is factory-set and read-only. The unique ID value can be used in conjunction with user software methods to help prevent illegal copying or cloning of a system.

Table 2: **Identification Definitions**

Command	Byte	Description	Value	Read Command
Manufacture ID	1	Manufacture ID	94h	9Eh/9Fh, AFh
Device ID	2	Memory Type ID	BBh	9Eh/9Fh, AFh
	3	Memory Capacity ID	20h	9Eh/9Fh, AFh
Unique ID	4	Number of remaining ID bytes	10h	9Eh/9Fh, AFh
	5	Extended device ID	See *Table **3***.	9Eh/9Fh, AFh
	6	Device configuration information	00h	9Eh/9Fh, AFh
	7:20	Unique ID Code (UID)	Customized data.	9Eh/9Fh, AFh

Table 3: **Extended Device ID Definition**

Bit	Description
Bit 7	Reserved.
Bit 6	Device generation, 0 = 1st generation.
Bit 5	0 = Standard BP scheme. 1 = Alternate BP scheme.
Bit 4	Reserved
Bit 3	HOLD#/RESET#: 0 = HOLD 1 = RESET
Bit 2	Additional Hardware RESET#: 0 = Not available. 1 = Available.
Bit 1	Sector size: 00 = Uniform 64KB.
Bit 0	

6.2. 3-Byte and 4-Byte Address Modes

The device supports both 3-byte and 4-byte address modes: 3-byte address mode can access a memory space of 128Mb, while 4-byte address mode allows the user to access memory space beyond 128Mbit.

Address mode is determined by SEL128 bit, ADP bit, Enter 4-Byte Address Mode command, and Exit 4-Byte Address Mode command.

SEL128 bit determines which 128Mbit segment to access for 3-byte address commands. ADP bit selects 3-byte or 4-byte mode; besides, when ADP is 1, the Extended Address Register allows the user to access memory space beyond 128Mbit.

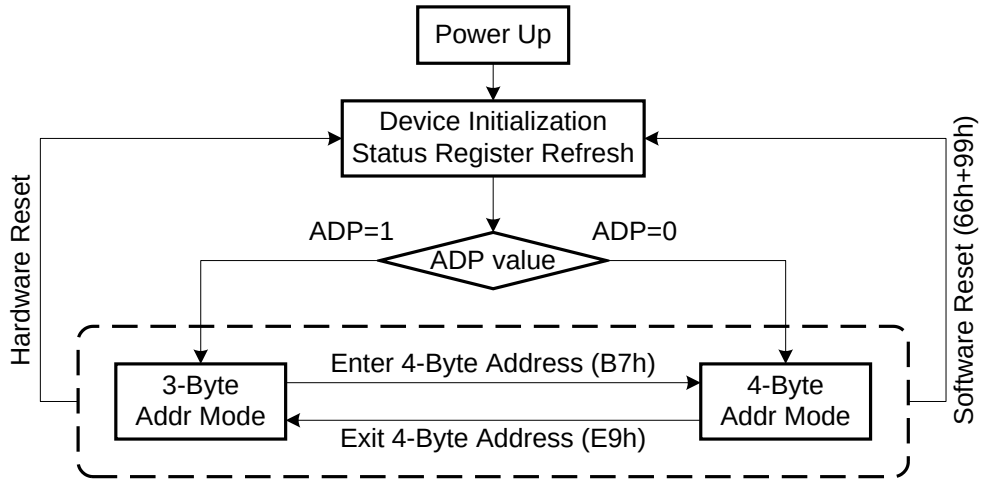


Figure 4: **ADP and Conversion between Address Modes**

6.3. Main Array Organization

The address space distribution for the main memory array is given below.

Table 4: **NM25LQ512A Memory Organization**

A device has	A 64KB Sector has	A 32KB Subsector has	A 4KB Subsector has	A page has	—
1024 (1K)	—	—	—	—	64KB Sector
2048 (2K)	2	—	—	—	32KB Subsector
16384 (16K)	16	8	—	—	4KB Subsector
262144 (256K)	256	128	16	—	Pages
67108864 (64M)	65536	32768	4096	256	Bytes

All blocks or sectors of the memory are of uniform size; the address distribution of NM25LQ512A is offered below.

Table 5: **NM25LQ512A Address Distribution**

Chip Capacity	64KB Sector	32KB Subsector	4KB Subsector	Address Range
512M bit or 64M byte	1023	2047	16383	03FF_F000h ~ 03FF_FFFFh
			……	……
			16376	03FF_8000h ~ 03FF_8FFFh
		2046	16375	03FF_7000h ~ 03FF_7FFFh
			……	……
			16368	03FF_0000h ~ 03FF_0FFFh
	……	……	……	……
	511	1023	8191	01FF_F000h ~ 01FF_FFFFh
			……	……
			8184	01FF_8000h ~ 01FF_8FFFh
		1022	8183	01FF_7000h ~ 01FF_7FFFh
			……	……
			8176	01FF_0000h ~ 01FF_0FFFh
	……	……	……	……
	255	511	4095	00FF_F000h ~ 00FF_FFFFh
			……	……
			4088	00FF_8000h ~ 00FF_8FFFh
		510	4087	00FF_7000h ~ 00FF_7FFFh
			……	……
			4080	00FF_0000h ~ 00FF_0FFFh
	……	……	……	……
	1	3	31	0001_F000h ~ 0001_FFFFh
			……	……
			24	0001_8000h ~ 0001_8FFFh
		2	23	0001_7000h ~ 0001_7FFFh
			……	……
			16	0001_0000h ~ 0001_0FFFh
	0	1	15	0001_F000h ~ 0001_FFFFh
			……	……
			8	0000_8000h ~ 0000_8FFFh
		0	7	0000_7000h ~ 0000_7FFFh
			……	……
			0	0000_0000h ~ 0000_0FFFh

6.4. State Table

At any given time, the device can only be in a specific state. In each certain state, some commands are accepted by the device while others are not. The following table summarizes the operations allowed during each state of the device.

Table 6: **Operations Allowed in Each Device State**

Operation	Standby State	Program or Erase State	Erase Suspend State or Program Suspend State	Note
Read (memory)	Yes	No	Yes	1
Read (status/flag status registers)	Yes	Yes	Yes	6
Program	Yes	No	Yes/No	2
Erase (Subsector, Sector, Bulk)	Yes	No	No	3
Write	Yes	No	No	4
Write	Yes	No	Yes	5
Suspend	No	Yes	No	7

Notes:

1. Read Status Register and Read Flag Register commands are not included.
2. Program OTP command is not included.
   Program operation on a sector other than the one in Erase suspension is allowed (Yes), otherwise it is not allowed (No).
3. Applies to: 4KB/32KB Subsector Erase, 64KB Sector Erase operations.
4. Applies to: Write Status Register, Write Nonvolatile Configuration Register, Program OTP, Bulk Erase.
5. Applies to: Write Volatile Configuration Register, Write Enhanced Volatile Configuration Register, Write Enable, Write Disable, Clear Flag Status Register, Write Extended Address Register, or Write Lock Register.
6. Applies to: Read Status Register, Read Flag Status Register.
7. Applies to: Program Suspend, Erase Suspend.

6.5. XIP Mode

Execute-In-Place (XIP) is a mode in which the random read access time is reduced by eliminating the command byte overhead, and simply sending the address bytes enables the device to output read data to the host. The XIP mode allows more flexibility in the application of the device.

6.5.1. Use Volatile Configuration Register to Activate/Terminate XIP Mode

After an application boots from SPI mode, it can switch to XIP mode by setting the XIP_EN bit of Volatile Configuration Register to 0 and then assert the XIP confirmation bit to 0 for the next Fast Read command. After the device is in XIP mode, subsequent commands will stay in the current SPI, DPI or QPI mode, and command bytes are no longer required.

Setting XIP confirmation bit to 1 terminates XIP mode.

6.5.2. Use Nonvolatile Configuration Register to Activate/Terminate XIP Mode

If directly booting from XIP mode is required, the host can write the Nonvolatile Configuration Register's XIP2, XIP1 and XIP0 bits to put the device into expected XIP mode. After the device powers up again, the device defaults to boot in XIP.

Setting XIP confirmation bit to 1 terminates XIP mode.

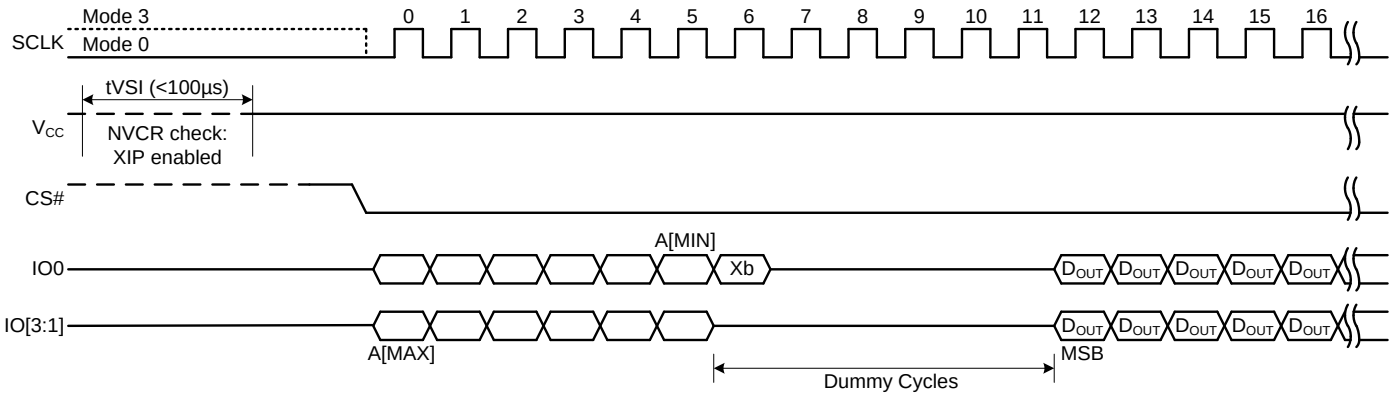


Figure 5: **Boot From XIP Mode**

6.5.3. XIP Confirmation Bit

XIP confirmation bit is defined as the value of IO0 in the first dummy clock cycle of the Fast Read operation in XIP mode. After XIP mode is enabled or disabled, this bit is used to activate or terminate XIP.

Table 7: **XIP Confirmation Bit**

Value	Description
0	Activate XIP.
1	Terminate XIP.

7. Data Protection

As a nonvolatile memory device the NM25LQ512A may suffer from the compromise of data integrity in the event of noise and other adverse system conditions. To improve the robustness of the device, certain methods are adopted to protect the data from inadvertent Write, Program or Erase operations.

7.1. Write Protect Features

NM25LQ512A offers the following protection schemes.

(1) The device is reset when Vcc is below threshold.

(2) Write is disabled for a duration after device is power-up.

(3) Prior to Write, Program or Erase operations, a Write Enable (WREN) command is needed to set WEL bit to 1; after these operations are complete, the WEL bit returns to 0.
This mechanism ensures that the memory content can be changed only after specific command sequence is successfully completed.

(4) Software Protection Mode:
A combination of Sector Protection registers and bits define the protection scheme on the basis of sectors. For details, see Section *7.3 Sector Protection*.
Also, the TB, BP3, BP2, BP1 and BP0 bits can be used to define the address space in the main memory array that is under protection. The protected area can only be read out; program or erase operations to protected area are ignored. For details, see Section *Table **13**:* NM25LQ512A Memory Protection Pattern.

(5) Hardware Protection Mode: WP# pin and SRP0 bit protect Status Register bits from modifications.
For details, see *Table 8*.

(6) While in Deep Power-Down Mode, the device ignores all commands except Release from Deep Power-Down Mode (ABh). This protects the device from all Write, Program or Erase commands.

7.2. Status Register Protection

SRP0 bits in the Status Register and WP# pin provide protection for the Status Register itself.

Table 8: **Status Register Protection Scheme**

SRP0	WP#	Protection Scheme	Description
0	x	Software Protected	Status Register is unlocked and can be written to after a Write Enable command which Sets WEL=1.(Default)
1	0	Hardware Protected	Status Register is locked and cannot be written to.
1	1	Hardware Unprotected	Status Register is unlocked and can be written to after a Write Enable command which Sets WEL=1.

7.3. Sector Protection

A combination of nonvolatile and volatile registers and bits allow sector and password protection to be implemented on various levels, as is presented below.

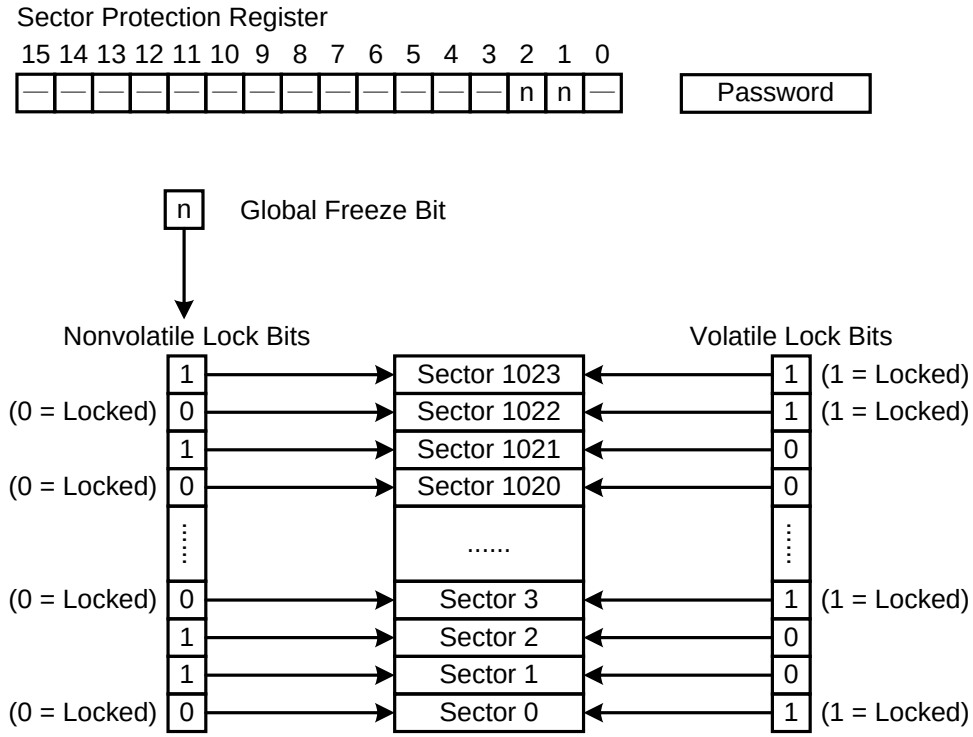


Figure 6: **Sector and Password Protection**

7.3.1. Sector Protection Register

The Sector Protection Register has 16 bits, and only bits 2 and 1 are active. This register is nonvolatile and one time programmable (OTP).

Table 9: **Sector Protection Register**

Bit	Name	Description	Volatility
15:3	Reserved	1 = Default.	—
2	Password Protection Lock	0 = Password protection is permanently enabled, and the 64-bit password cannot be read or modified. 1 = Password protection is disabled. (Default)	Nonvolatile OTP
1	Sector Protection Lock	0 = Nonvolatile lock bits can be modified. In this case, bit 2 must be set to 1. 1 = Nonvolatile lock bits can be modified. In this case, bit 2 can be 0 or 1. (Default).	Nonvolatile OTP
0	Reserved	1 = Default.	—

The sector protection register is written by 2Ch and read by 2Dh commands. Write operation is permanent and irreversible. Once written from 1 to 0, it cannot be written back to 1. PL/SL is exclusive that only one can be set to 0. If you write PL/SL 2'b00 will be set 2'b01. The password must program before Password Protection Lock bit is set to 0 otherwise you will get a confused password. When Password Protection Lock bit is set to 0, the global freeze bit will become 0 after reset and you can't write nonvolatile lock bits registers. You should send corrected password to unlock password protection that set global freeze bit to 1. Whether Sector Protection Lock bit is set to 0 or 1, it enables write nonvolatile lock bits registers.

7.3.2. Global Freeze Bit

The Global Freeze Bit is used to protect the contents of Nonvolatile Lock Bits.

Table 10: **Global Freeze Bit Register**

Bit	Name	Description	Volatility
7:1	Reserved	0 = Default.	—
0	Global Freeze Bit	0 = Nonvolatile lock bits are protected against Program or Erase operations. 1 = Nonvolatile lock bits can be modified by Program or Erase operations. (Default)	Volatile

This register is written by A6h and read by A7h commands.

When password protection is disabled, the Write Global Freeze Bit A6h command can change this bit from 1 to 0, or from 0 to 1. When password protection is enabled, the A6h command can only change this bit from 1 to 0, but not the reverse; in such case, in order to change the Global Freeze Bit from 0 to 1, an Unlock Password 29h command together with the expected 64-bit password is needed.

7.3.3. Nonvolatile Lock Bits

The device has 1024 Nonvolatile Lock Bits, each corresponding to a specific sector of the main memory array.

Table 11: **Nonvolatile Lock Bits**

Bit	Name	Description	Volatility
1023	Nonvolatile Lock Bit	0 = Enable lock; protects Sector 1023 from Program or Erase operations. 1 = Disable lock; protection of Sector 1023 is disabled.	Nonvolatile
1022	Nonvolatile Lock Bit	0 = Enable lock; protects Sector 1022 from Program or Erase operations. 1 = Disable lock; protection of Sector 1022 is disabled.	Nonvolatile
.....	.....	.....	.....
1	Nonvolatile Lock Bit	0 = Enable lock; protects Sector 1 from Program or Erase operations. 1 = Disable lock; protection of Sector 1 is disabled.	Nonvolatile
0	Nonvolatile Lock Bit	0 = Enable lock; protects Sector 0 from Program or Erase operations. 1 = Disable lock; protection of Sector 0 is disabled.	Nonvolatile

These bits are read, written and erased by E2h, E3h and E4h commands, respectively. A Write operation sets a specific bit to 0, while an Erase operation simultaneously clears all Nonvolatile Lock Bits to 1.

7.3.4. Volatile Lock Bit Register

The device has 1054 Volatile Lock Bit Registers, each corresponding to a specific sector of the main memory array.

The first and last sectors will have volatile protections at the 4KB subsector level. Each 4KB subsector in these sectors can be individually locked by volatile lock bits setting. All volatile lock bit registers share one Sector Lock Down bit.

Table 12: **Volatile Lock Bit Registers**

Register	Bit	Name	Description	Volatility

1053	7:2	Reserved	Reserved bits are 0.	—
	1	Sector Lock Down	0 = Disable lock-down (default); bits [1] and [0] can be written to 1. 1 = Enable lock-down; bits [1] and [0] are protected against write operations until power-down or reset.	Volatile
	0	Sector Write Lock	0 = Disable write lock (default); Sector 1053 can be Programmed or Erased. 1 = Enable write lock; Sector 1053 is protected against Program or Erase operations.	Volatile
.....	.....	.....	.....	.....
0	7:2	Reserved	Reserved bits are 0.	—
	1	Sector Lock Down	0 = Disable lock-down (default); bits [1] and [0] can be written to 1. 1 = Enable lock-down; bits [1] and [0] are protected against write operations until power-down or reset.	Volatile
	0	Sector Write Lock	0 = Disable write lock (default); Sector 0 can be Programmed or Erased. 1 = Enable write lock; Sector 0 is protected against Program or Erase operations.	Volatile

These bits are read by E5h/E1h, and written by E8h/E0h commands.

7.4. Password Protection

The device has an internal password that is read, written and unlocked by 27h, 28h and 29h commands, respectively.

In the NM25LQ512A device, the Sector Protection Register is used to enable or disable password protection mechanism, and such mechanism is used to prevent the Global Freeze Bit from unauthorized modifications.

The host may set and verify the password using 28h and 27h commands, respectively. If the password is set and password protection is enabled, then an Unlock Password 29h command together with the expected 64-bit password can reset the Global Freeze Bit to 1.

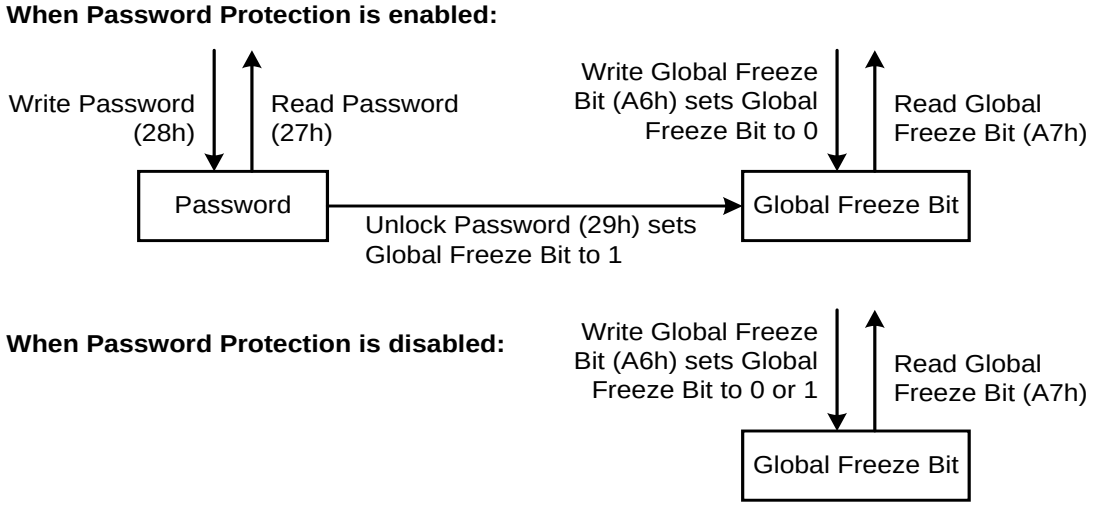


Figure 7: **Password Protection and Global Freeze Bit**

7.5. Main Memory Array Protection

A combination of Status Register bits define the area space of the memory array that is protected from program

and erase operations. A program operation targeted at a page address that is under protection is not executed. For erase operations, if any address location within the designated target area is protected, then the command is not executed.

Table 13: **NM25LQ512A Memory Protection Pattern**

Status Register Bits					Memory Space in Protection	
TB	BP3	BP2	BP1	BP0	Address	Density
X	0	0	0	0	NONE	NONE
0	0	0	0	1	03FF_0000h ~ 03FF_FFFFh	64KByte
0	0	0	1	0	03FE_0000h ~ 03FF_FFFFh	128KByte
0	0	0	1	1	03FC_0000h ~ 03FF_FFFFh	256KByte
0	0	1	0	0	03F8_0000h ~ 03FF_FFFFh	512KByte
0	0	1	0	1	03F0_0000h ~ 03FF_FFFFh	1MByte
0	0	1	1	0	03E0_0000h ~ 03FF_FFFFh	2MByte
0	0	1	1	1	03C0_0000h ~ 03FF_FFFFh	4MByte
0	1	0	0	0	0380_0000h ~ 03FF_FFFFh	8MByte
0	1	0	0	1	0300_0000h ~ 03FF_FFFFh	16MByte
0	1	0	1	0	0200_0000h ~ 03FF_FFFFh	32MByte
1	0	0	0	1	0000_0000h ~ 0000_FFFFh	64KByte
1	0	0	1	0	0000_0000h ~ 0001_FFFFh	128KByte
1	0	0	1	1	0000_0000h ~ 0003_FFFFh	256KByte
1	0	1	0	0	0000_0000h ~ 0007_FFFFh	512KByte
1	0	1	0	1	0000_0000h ~ 000F_FFFFh	1MByte
1	0	1	1	0	0000_0000h ~ 001F_FFFFh	2MByte
1	0	1	1	1	0000_0000h ~ 003F_FFFFh	4MByte
1	1	0	0	0	0000_0000h ~ 007F_FFFFh	8MByte
1	1	0	0	1	0000_0000h ~ 00FF_FFFFh	16MByte
1	1	0	1	0	0000_0000h ~ 01FF_FFFFh	32MByte
X	1	1	X	X	0000_0000h ~ 03FF_FFFFh	64MByte
X	1	0	1	1	0000_0000h ~ 03FF_FFFFh	64MByte

8. Device Registers

8.1. Status Register

Table 14: **Status Register**

Bit	Name	Description	Volatility	R/W
7	SRP0	Status register protect 0.	Nonvolatile	Writable
6	TB	Top/bottom protect.	Nonvolatile	Writable
5	BP3	Block protect bit.	Nonvolatile	Writable
4	BP2	Block protect bit.	Nonvolatile	Writable
3	BP1	Block protect bit.	Nonvolatile	Writable
2	BP0	Block protect bit.	Nonvolatile	Writable
1	WEL	Write enable latch.	Volatile	Read only
0	WIP	Write in process.	Volatile	Read only

The Status Register is read by 05h and written by 01h commands.

8.1.1. SRP0 Bit

Status Register Protect Bit (SRP0) and WP# pin determine the protection scheme of Status Register.

0 = Enabled(Default)

1 = Disabled

For details, see *Table **8**:* Status Register Protection Scheme.

8.1.2. TB Bit

Top/Bottom Protect bit determines whether the memory protection mechanism starts from the Top or Bottom address of the memory array.

0 = Top (Default)

1 = Bottom

TB bit and Block Protect bits (BP3 through BP0) together determine the exact protection scheme of the main memory array. For details, see *Table **13**:* NM25LQ512A Memory Protection Pattern.

8.1.3. BP3, BP2, BP1, BP0 Bits

BP3 through BP0 are Block Protect bits. They specify the protected memory space in the main memory array, default value is 4'b0.

For details, see *Table **13**:* NM25LQ512A Memory Protection Pattern.

8.1.4. WEL Bit

Write Enable Latch Bit(WEL) indicates whether the device is ready to accept an incoming Write, Program or Erase command:

0 = Clear (Default)

1 = Set

This bit is reset by:

(1) Power up;

(3) Write Disable (WRDI, 04h) command;

(2) Completion of Write, Program or Erase operations;

(4) Software Reset (66h+99h) command.

8.1.5. WIP Bit

Write In Progress Bit(WIP) indicates whether a Write, Program or Erase operation is in progress.

0 = Device is Ready (Default)

1 = Device is Busy in Write, Program or Erase operation.

8.2. Flag Status Register

Table 15: **Flag Status Register**

Bit	Name	Description	Volatility	R/W
7	RY/BY#	Program or Erase Ready/Busy# Status Bit.	Volatile	Read only
6	SUS1	Erase Suspend Status.	Volatile	Read only
5	EE	Erase Error Bit.	Volatile	Read only
4	PE	Program Error Bit.	Volatile	Read only
3	Reserved	Reserved.	—	—
2	SUS2	Program Suspend Status.	Volatile	Read only
1	PTE	Protection Error bit.	Volatile	Read only
0	ADS	Current Address Mode.	Volatile	Read only

The Flag Status Register is read by 70h command. This register is read only and cannot be written. The power-up

default value of this register is 80h.

8.2.1. RY/BY# Bit

The RY/BY# bit indicates the status of a Program or Erase operation, signifying whether anyone of the following operations is in progress: Write Status Register, Write Nonvolatile Configuration Register, Program, Erase.

0 = Busy

1 = Ready(default)

8.2.2. SUS2, SUS1 Bits

SUS2: Program Suspend Bit indicates whether a Program operation is in suspension. The bit is set to 1 by 75h command, cleared to 0 by 7Ah or 66h+99h commands, or by powering up the device.

0 = The device is not in Program suspension.

1 = Program suspension in progress.

SUS1: Erase Suspend Bit indicates whether an Erase operation is in suspension. The bit is set to 1 by 75h command, cleared to 0 by 7Ah or 66h+99h commands, or by powering up the device.

0 = The device is not in Erase suspension.

1 = Erase suspension in progress.

8.2.3. EE Bit

Erase Error Bit(EE) is a read only bit that is set to 1 when an erase failure occurs, or when the user attempts to erase a protected address or OTP area.

This bit is cleared by Clear Flag Status Register (50h) command, new successful erase command or reset.

0 = Clear.

1 = Failure or protection error.

8.2.4. PE Bit

Program Error Bit(PE) is a read only bit that is set to 1 when a program failure occurs, or when the user attempts to program a protected address or OTP area.

This bit is cleared by Clear Flag Status Register (50h) command, new successful program command or reset.

0 = Clear.

1 = Failure or protection error.

8.2.5. PTE Bit

The Protection Error Bit (PTE) is asserted when a Program or Erase operation is attempted on a protected area, or when a Program operation is attempted on a locked OTP space.

This bit is cleared by Clear Flag Status Register (50h) command.

0 = Clear

1 = Failure or protection error

8.2.6. ADS Bit

Address Status bit is a read only bit that indicates the address mode.

0 = The device is in 3-byte address mode (default).

1 = The device is in 4-byte address mode.

8.3. Extended Address Register

In 3-byte address mode, the A[23:0] address provided in a command sequence can access a memory space of only 128Mbit. However, it is possible to access the full address range of the device in 3-byte address mode with Extended Address Register, which provides the higher address bits A[25:24] and allows the user to access address space beyond 128Mbit in 3-byte address mode.

Table 16: **Extended Address Register**

Bit	Name	Description	Volatility	R/W
7	A[31]	Reserved.	—	—
6	A[30]	Reserved.	—	—
5	A[29]	Reserved.	—	—
4	A[28]	Reserved.	—	—
3	A[27]	Reserved.	—	—
2	A[26]	Reserved.	—	—
1	A[25]	Address bit.	Volatile	Writable
0	A[24]	Address bit.	Volatile	Writable

The Extended Address Register is read by C8h and written by C5h commands.

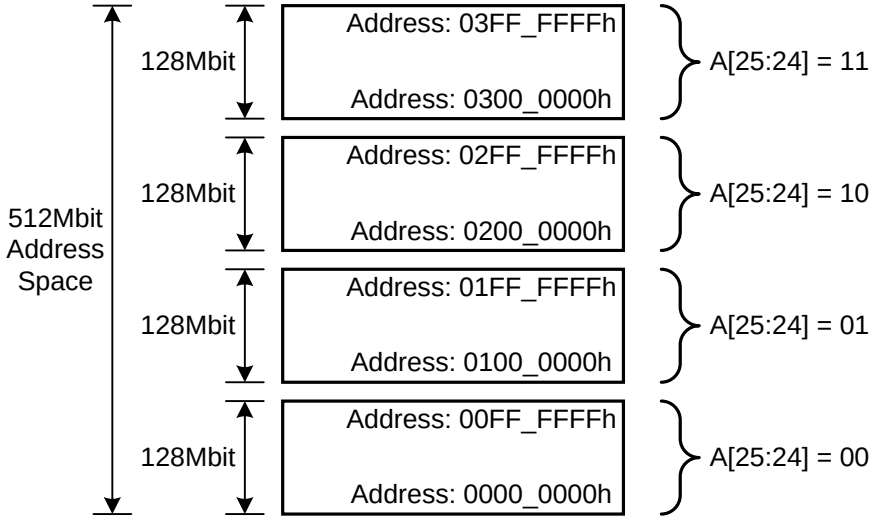


Figure 8: **Address Space Segments**

8.4. OTP Area Security Register

The 512-byte OTP Area Security Registers of the device can be individually read, programmed using 4Bh, 42h commands. The host may use Security Registers to store security or other important information separately from the main memory array.

The OTP area Security Registers can be individually protected by OTP programmable LB bit. Once a LB bit is set to 0, the corresponding Security Register becomes permanently locked and all program operations are ignored.

Table 17: **Security Register Address Distribution**

Security Register	Address Bits 23-16	Address Bits 15-12	Address Bits 11-8	Address Bits 7-0
Security Register	X, X, X, X, X, X, X, X	X, X, X, X	X, X, X, A8	A7, A6, ..., A1, A0

Notes:

1. The address bits "X" are don't care.

8.5. SFDP Register

The NM25LQ512A features a 256-byte Serial Flash Discovery Parameter (SFDP) register. It provides a means to interrogate flash device characteristics and make appropriate adjustments while accessing the device.

The concept of SFDP Register definitions is similar to the JEDEC JESD216 standard (April 2011).

8.5.1. SFDP Header Information

Table 18: **Signature and Parameter Identification Data Values**

Description	Comment	Addr[1]	Bits[2]	Data[3]	Data[4]
SFDP Signature		00h	[07:00]	53h	53h
		01h	[15:08]	46h	46h
		02h	[23:16]	44h	44h
		03h	[31:24]	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	[07:00]	06h	06h
SFDP Major Revision Number	Start from 01h	05h	[15:08]	01h	01h
Number of Parameters Headers	Start from 00h	06h	[23:16]	01h	01h
Unused	Contains 0xFFh and can never be changed	07h	[31:24]	FFh	FFh
ID number (JEDEC)	00h: A JEDEC specified header	08h	[07:00]	00h	00h
Parameter Table Minor Revision Number	Start from 0x00h	09h	[15:08]	06h	06h
Parameter Table Major Revision Number	Start from 0x01h	0Ah	[23:16]	01h	01h
Parameter Table Length (in double word)	Number of DWORDs in the Parameter table	0Bh	[31:24]	10h	10h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	[07:00]	30h	30h
		0Dh	[15:08]	00h	00h
		0Eh	[23:16]	00h	00h
Unused	Contains 0xFFh and can never be changed.	0Fh	[31:24]	FFh	FFh
ID Number (NeuMem Manufacturer ID)	Indicates NeuMem manufacturer ID	10h	[07:00]	94h	94h
Parameter Table Minor Revision Number	Start from 0x00h	11h	[15:08]	00h	00h
Parameter Table Major Revision Number	Start from 0x01h	12h	[23:16]	01h	01h
Parameter Table Length (in double word)	Number of DWORDs in the Parameter table	13h	[31:24]	02h	03h
Parameter Table Pointer (PTP)	First address of NeuMem Flash Parameter table	14h	[07:00]	80h	60h
		15h	[15:08]	00h	00h
		16h	[23:16]	00h	00h
Unused	Contains 0xFFh and can never be changed	17h	[31:24]	FFh	FFh

Notes:

1. The "Addr" column indicates the byte address in SFDP area.
2. The "Bits" column is the bit range of the specified data within a 32-bit-word which comprises four consecutive 8-bit bytes.
3. This column is the data expressed in binary (with suffix "b") or hexadecimal (with suffix "h").
4. This column is the data in hexadecimal, as is indicated by the suffix "h".

8.5.2. Parameter Table (0)

Table 19: **Parameter Table (0): JEDEC Flash Parameter Tables**

Description	Comment	Addr	Bits	Data	Data

Block/Sector Erase Size	00: Reserved; 01: 4KB Erase; 10: Reserved; 11: do not support 4KB erase	30h	[01:00]	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		[02]	1b	
Write Enable Instruction Required for Writing to Volatile Status Register	0: Nonvolatile status bit 1: Volatile status bit		[03]	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50h Opcode; 1: Use 06h Opcode. Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		[04]	0b	
Unused	Contains 111b and can never be changed		[07:05]	111b	
4KB Erase Opcode		31h	[15:08]	20h	20h
(1-1-2) Fast Read	0=Not supported 1=Supported	32h	[16]	1b	FBh
Number of Address Bytes used in addressing flash array	00: 3-Byte only; 01: 3- or 4-Byte; 10: 4-Byte only; 11: Reserved		[18:17]	01b	
Double Transfer Rate (DTR) clocking	0=Not supported 1=Supported		[19]	1b	
(1-2-2) Fast Read	0=Not supported 1=Supported		[20]	1b	
(1-4-4) Fast Read	0=Not supported 1=Supported		[21]	1b	
(1-1-4) Fast Read	0=Not supported 1=Supported		[22]	1b	
Unused	—		[23]	1b	
Unused	—	33h	[31:24]	FFh	FFh
Flash Memory Density		37h: 34h	[31:00]	1FFF_FFFFh	
(1-4-4) Fast Read Number of Wait states	0_0000b: Wait states (dummy clocks) not supported	38h	[04:00]	0_1000b	29h
(1-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[07:05]	001b	
(1-4-4) Fast Read Opcode		39h	[15:08]	EBh	EBh
(1-1-4) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	3Ah	[20:16]	0_0111b	27h
(1-1-4) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[23:21]	001b	
(1-1-4) Fast Read Opcode		3Bh	[31:24]	6Bh	6Bh
(1-1-2) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	3Ch	[04:00]	0_0111b	27h

(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[07:05]	001b	
(1-1-2) Fast Read Opcode		3Dh	[15:08]	3Bh	3Bh
(1-2-2) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	3Eh	[20:16]	0_0111b	27h
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[23:21]	001b	
(1-2-2) Fast Read Opcode		3Fh	[31:24]	BBh	BBh
(2-2-2) Fast Read	0: Not supported 1: Supported	40h	[00]	1b	FFh
Unused	—		[03:01]	111b	
(4-4-4) Fast Read	0: Not supported 1: Supported		[04]	1b	
Unused	—		[07:05]	111b	
Unused	—	43h:41h	[31:08]	FF_FFFFh	FF_FFFFh
Unused	—	45h:44h	[15:00]	FFFFh	FFFFh
(2-2-2) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	46h	[20:16]	0_0111b	27h
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[23:21]	001b	
(2-2-2) Fast Read Opcode		47h	[31:24]	BBh	BBh
Unused	—	49h:48h	[15:00]	FFFFh	FFFFh
(4-4-4) Fast Read Number of Wait states	0_0000b: Wait states (Dummy Clocks) not supported	4Ah	[20:16]	0_1001b	29h
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not supported		[23:21]	001b	
(4-4-4) Fast Read Opcode		4Bh	[31:24]	EBh	EBh
Sector Type 1 Size	0x00b: Sector type doesn't exist N: sector/block size = 2^N bytes	4Ch	[07:00]	0Ch	0Ch
Sector Type 1 erase Opcode		4Dh	[15:08]	20h	20h
Sector Type 2 Size	0x00b: Sector type doesn't exist N: sector/block size = 2^N bytes	4Eh	[23:16]	10h	10h
Sector Type 2 erase Opcode		4Fh	[31:24]	D8h	D8h
Sector Type 3 Size	0x00b: Sector type doesn't exist N: sector/block size = 2^N bytes	50h	[07:00]	0Fh	0Fh
Sector Type 3 erase Opcode		51h	[15:08]	52h	52h
Sector Type 4 Size	0x00b: Sector type doesn't exist N: sector/block size = 2^N bytes	52h	[23:16]	00h	00h
Sector Type 4 erase Opcode		53h	[31:24]	00h	00h

8.5.3. Parameter Table (1)

Table 20: **Parameter Table (1): NeuMem Flash Parameter Tables**

Description	Comment	Addr	Bits	Data	Data

Vcc Supply Maximum Voltage	2000h=2.000V 2700h=2.700V 3600h=3.600V	61h: 60h	[15:00]	2000h	2000h
Vcc Supply Minimum Voltage	1650h=1.650V 2250h=2.250V 2350h=2.350V 2700h=2.700V	63h: 62h	[31:16]	1650	1650
HW Reset# pin	0 = Not supported 1 = Supported	65h: 64h	[00]	1b	F99Fh
HW Hold# pin	0 = Not supported 1 = Supported		[01]	1b	
Deep Power Down Mode	0 = Not supported 1 = Supported		[02]	1b	
Software Reset	0 = Not supported 1 = Supported		[03]	1b	
Software Reset Opcode	(Reset Enable 66h should be issued before Reset Opcode)		[11:04]	99h	
Program Suspend/Resume	0 = Not supported 1 = Supported		[12]	1b	
Erase Suspend/Resume	0 = Not supported 1 = Supported		[13]	1b	
Unused	—		[14]	1b	
Wrap-Around Read mode	0 = Not supported 1 = Supported		[15]	1b	
Wrap-Around Read mode Opcode		66h	[23:16]	77h	77h
Wrap-Around Read data length	08h: Support 8B wrap-around read 16h: 8B & 16B 32h: 8B & 16B & 32B 64h: 8B & 16B & 32B & 64B	67h	[31:24]	64h	64h
Individual block lock	0 = Not supported 1 = Supported	6Bh: 68h	[00]	0b	EBFCh
Individual block lock bit (Volatile/Nonvolatile)	0 = Volatile 1 = Nonvolatile		[01]	0b	
Individual block lock Opcode			[09:02]	FFh	
Individual block lock Volatile protect bit default protect status	0 = Protect 1 = Unprotect		[10]	0b	
Secured OTP	0 = Not supported 1 = Supported		[11]	1b	
Read Lock	0 = Not supported 1 = Supported		[12]	0b	
Permanent Lock	0 = Not supported 1 = Supported		[13]	1b	
Unused	—		[15:14]	11b	

Unused	—	[31:16]	FFFFh	FFFFh

9. Internal Configuration Register

9.1. Internal Configuration Register and Device Behavior

The NM25LQ512A device has an internal configuration register that define the memory configuration. This register is invisible to the user; rather, it is determined by internal volatile and nonvolatile configuration registers. The user can indirectly change internal configuration register value in the following ways:

1. The user uses the Write Nonvolatile Configuration Register command to modify the contents of the nonvolatile register. Afterwards, at power up or after a reset, information from nonvolatile configuration register is loaded into internal configuration register, thus changing the power-up default configuration.
2. The user uses the Write Volatile Configuration Register or Write Enhanced Volatile Configuration Register commands to modify the contents of these volatile registers. After these Write commands are finished, the information in these volatile configuration registers are immediately loaded into internal configuration register, thus changing the configuration while the device is operation.

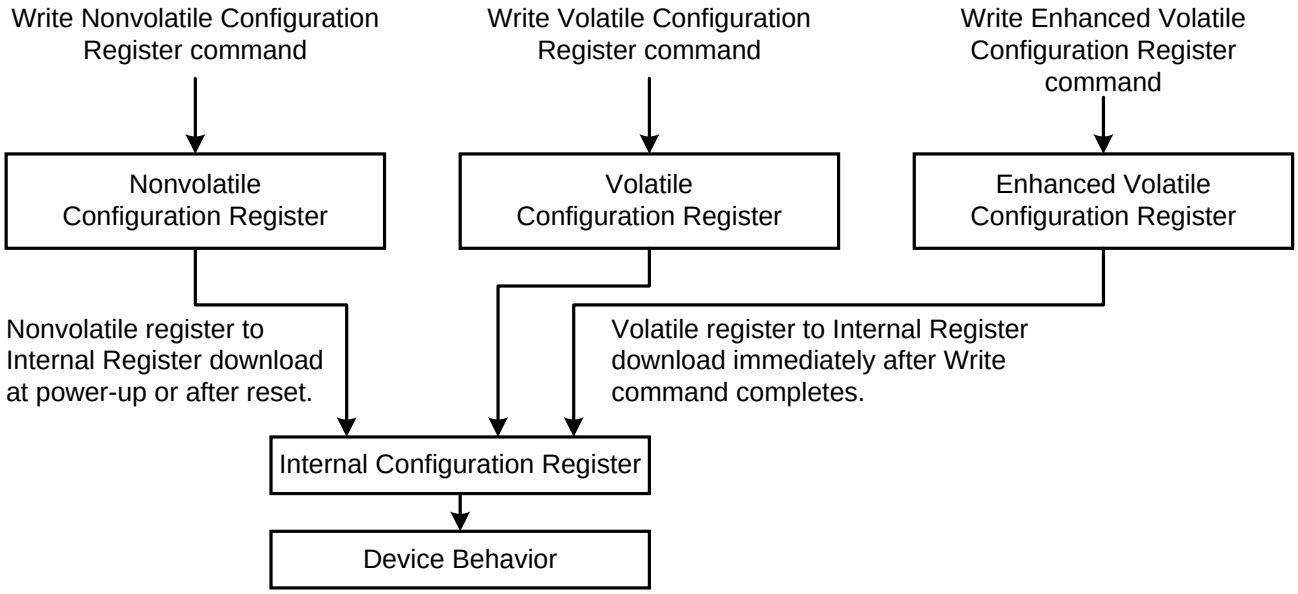


Figure 9: **Internal Configuration Register and Device Behavior**

9.2. Nonvolatile Configuration Register

Table 21: **Nonvolatile Configuration Register**

Bit	Name	Description	Volatility	R/W
15	DC3	Number of dummy clock cycles.	Nonvolatile.	Writable.
14	DC2	Number of dummy clock cycles.	Nonvolatile.	Writable.
13	DC1	Number of dummy clock cycles.	Nonvolatile.	Writable.
12	DC0	Number of dummy clock cycles.	Nonvolatile.	Writable.
11	XIP2	XIP mode at power-on reset.	Nonvolatile.	Writable.
10	XIP1	XIP mode at power-on reset.	Nonvolatile.	Writable.
9	XIP0	XIP mode at power-on reset.	Nonvolatile.	Writable.
8	Reserved.	Reserved.	Nonvolatile.	Writable.
7	DRV1	Output drive strength.	Nonvolatile.	Writable.
6	DRV0	Output drive strength.	Nonvolatile.	Writable.

5	DTRB	Double Transfer Rate (DTR) protocol.	Nonvolatile.	Writable.
4	HOLDRST	Reset/hold.	Nonvolatile.	Writable.
3	QPIB	Quad Peripheral Interface (QPI) protocol.	Nonvolatile.	Writable.
2	DPIB	Dual Peripheral Interface (DPI) protocol.	Nonvolatile.	Writable.
1	SEL128	128Mb segment.	Nonvolatile.	Writable.
0	ADP	Address Powerup bit.	Nonvolatile.	Writable.

This register is read by B5h and written by B1h commands.

9.2.1. DC3, DC2, DC1, DC0 Bits

These bits specify the number of dummy clock cycles after all Fast Read commands.

0000 = Identical to 1111
0001 = Identical to 1111
0010 = Identical to 1111
0011 = 3 dummy clock cycles
⋮
1101 = 13 dummy clock cycles
1110 = 14 dummy clock cycles
1111 = Default

9.2.2. XIP2, XIP1, XIP0 Bits

These bits specify the XIP mode of the device. They takes effect after device is power-up.

000 = XIP: Fast read
001 = XIP: Dual output fast read
010 = XIP: Dual Input/Output fast read
011 = XIP: Quad output fast read
100 = XIP: Quad Input/Output fast read
101 = Reserved
110 = Reserved
111 = Disabled (Default)

9.2.3. DRV1, DRV0 Bits

DRV1 and DRV0 Bits determine the drive strength of output buffers in read operations.

DRV1, DRV0 = 00: 100%
DRV1, DRV0 = 01: 75%
DRV1, DRV0 = 10: 50%
DRV1, DRV0 = 11: 25%(Default)

9.2.4. DTRB Bit

The DTRB bit enables the device to operate in Double Transfer Rate protocol. After DTR bit is set to 0, all subsequent commands are in DTR mode.

0 = Enabled
1 = Disabled (Default)

9.2.5. HOLDRST Bit

The HOLDRST bit enables or disables the HOLD# or RESET# functions on IO3 pin.

0 = Disabled
1 = Enabled(Default)

9.2.6. QPIB Bit

The QPIB bit selects whether the device works in Quad Peripheral Interface (QPI) mode.

0 = Enabled

1 = Disabled (Default)

9.2.7. DPIB Bit

The DPIB bit selects whether the device works in Dual Peripheral Interface (DPI) mode.

0 = Enabled

1 = Disabled (Default)

9.2.8. SEL128 Bit

The 512Mbit memory space of a NM25LQ512A device can be further divided into four 128Mbit segments. The SEL128 bit selects the power-up default segment to access for 3-byte address commands.

0 = Highest 128Mb segment

1 = Lowest 128Mb segment (Default)

9.2.9. ADP Bit

Address Powerup bit specifies the initial address mode upon device power up or after reset.

0 = 4-byte address mode after power up.

1 = 3-byte address mode after power up (Default).

9.3. Volatile Configuration Register

Table 22: **Volatile Configuration Register**

Bit	Name	Description	Volatility	R/W
7	DC3	Number of dummy clock cycles.	Volatile.	Writable.
6	DC2	Number of dummy clock cycles.	Volatile.	Writable.
5	DC1	Number of dummy clock cycles.	Volatile.	Writable.
4	DC0	Number of dummy clock cycles.	Volatile.	Writable.
3	XIP_EN	XIP mode.	Volatile.	Writable.
2	Reserved.	Reserved.	Volatile.	Writable.
1	WRAP1	Wrap control bit.	Volatile.	Writable.
0	WRAP0	Wrap control bit.	Volatile.	Writable.

This register is read by 85h and written by 81h commands.

9.3.1. DC3, DC2, DC1, DC0 Bits

See *9.2.1 DC3, DC2, DC1, DC0 Bits*.

9.3.2. XIP_EN Bit

This bit enables or disables the XIP function of the device.

0 = Enabled

1 = Disabled (Default)

9.3.3. WRAP1, WRAP0 Bits

The Wrap Bits specify the wrap around mode of read operations. For N-byte wrap mode, the read operation is limited within an N-byte address boundary, starting from the 3-byte address specified by the command sequence.

00 = 16-byte boundary aligned

01 = 32-byte boundary aligned

10 = 64-byte boundary aligned

11 = Continuous (Default)

Address wrapping pattern is detailed in *Table **23*** through *Table **25***:

Table 23: **Address Wrapping Pattern for 16-Byte Wrap**

Starting Address Bits [3:0]	Wrapping Pattern
0	0-1-2- ..... -15-0-1- .....
1	1-2- ..... -15-0-1-2- .....
.....	.....
15	15-0-1-2-3- ..... -15-0-1- .....

Table 24: **Address Wrapping Pattern for 32-Byte Wrap**

Starting Address Bits [4:0]	Wrapping Pattern
0	0-1-2- ..... -31-0-1- .....
1	1-2- ..... -31-0-1-2- .....
.....	.....
15	15-16-17- ..... -31-0-1- .....
.....	.....
31	31-0-1-2-3- ..... -31-0-1- .....

Table 25: **Address Wrapping Pattern for 64-Byte Wrap**

Starting Address Bits [5:0]	Wrapping Pattern
0	0-1-2- ..... -63-0-1- .....
1	1-2- ..... -63-0-1-2- .....
.....	.....
15	15-16-17- ..... -63-0-1- .....
.....	.....
31	31-32-33- ..... -63-0-1- .....
.....	.....
63	63-0-1- ..... -63-0-1- .....

9.4. Enhanced Volatile Configuration Register

Table 26: **Enhanced Volatile Configuration Register**

Bit	Name	Description	Volatility	R/W
7	QPIB	Quad Peripheral Interface (QPI) protocol.	Volatile.	Writable.
6	DPIB	Duad Peripheral Interface (DPI) protocol.	Volatile.	Writable.
5	DTRB	Double Transfer Rate (DTR) protocol.	Volatile.	Writable.
4	HOLDRST	Reset/hold.	Volatile.	Writable.
3	Reserved.	Reserved.	—	—
2	DRV1	Output drive strength.	Volatile.	Writable.
1	DRV0	Output drive strength.	Volatile.	Writable.
0	Reserved.	Reserved.	—	—

This register is read by 65h and written by 61h commands.

See *9.2 Nonvolatile Configuration Register* for detailed description of these bits.

9.5. Supported Clock Frequencies

The highest clock frequency that the device supports is dependent on the number of dummy clock cycles, as is shown below:

Table 27: **Clock Frequency and Number of Dummy Clock Cycles-STR for IT and AT part**

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
0	Default	Default	Default	Default	Default
1	Default	Default	Default	Default	Default
2	Default	Default	Default	Default	Default
3	129	106	86	Default	Default
4	146	115	97	97	69
5	162	125	106	106	78
6	166	134	115	115	86
7	166	143	125	125	97
8	166	152	134	134	106
9	166	162	143	143	115
10	166	166	152	152	125
11	166	166	162	162	134
12	166	166	166	166	143
13	166	166	166	166	156
14	166	166	166	166	166

Table 28: **Clock Frequency and Number of Dummy Clock Cycles-STR for UT part**

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
0	Default	Default	Default	Default	Default
1	Default	Default	Default	Default	Default
2	Default	Default	Default	Default	Default
3	129	106	86	Default	Default
4	146	115	97	97	69
5	162	125	106	106	78
6	166	134	115	115	86
7	166	143	125	125	97
8	166	152	134	133	106
9	166	162	143	133	115
10	166	166	152	133	125
11	166	166	162	133	133
12	166	166	166	133	133
13	166	166	166	133	133
14	166	166	166	133	133

Table 29: **Clock Frequency and Number of Dummy Clock Cycles-DTR for IT and AT part**

Number of Dummy Clock	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ

Cycles					
0	Default	Default	Default	Default	Default
1	Default	Default	Default	Default	Default
2	Default	Default	Default	Default	Default
3	82	68	59	Default	Default
4	90	76	65	65	49
5	90	83	75	75	58
6	90	90	83	83	68
7	90	90	90	90	78
8	90	90	90	90	85
9	90	90	90	90	90
10	90	90	90	90	90
11	90	90	90	90	90
12	90	90	90	90	90
13	90	90	90	90	90
14	90	90	90	90	90

Table 30: **Clock Frequency and Number of Dummy Clock Cycles-DTR for UT part**

Number of Dummy Clock Cycles	FAST READ	DUAL OUTPUT FAST READ	DUAL I/O FAST READ	QUAD OUTPUT FAST READ	QUAD I/O FAST READ
0	Default	Default	Default	Default	Default
1	Default	Default	Default	Default	Default
2	Default	Default	Default	Default	Default
3	82	68	59	Default	Default
4	90	76	65	65	49
5	90	83	75	75	58
6	90	90	83	80	68
7	90	90	90	80	78
8	90	90	90	80	80
9	90	90	90	80	80
10	90	90	90	80	80
11	90	90	90	80	80
12	90	90	90	80	80
13	90	90	90	80	80
14	90	90	90	80	80

10. Command Definitions

All commands, addresses and data are shifted in and out of the device, beginning with the MSB of the command byte.

Every command sequence starts with a one-byte command code. Depending on the operation, the command byte might be followed by address bytes, data bytes, dummy bytes, or their combination. CS# must be driven high after the last bit of the command sequence is completed.

Read-related commands (Read, Fast Read, Read Register, Read Device ID) shifts out data from the device. CS# can be driven high after any bit of the output data sequence.

For other commands including Page Program, Subsector Erase, Sector Erase, Bulk Erase, Write Status Register,

Write Enable, Write Disable or Deep Power-Down, CS# must be driven high exactly at a byte boundary; otherwise if CS# is driven high at any time when the input byte is not a full byte, the command is ignored and WEL will not be reset.

10.1. Command Summary

Standard SPI, DPI and QPI interface protocols use 1, 2 and 4 pins to communicate command code, respectively. The number of pins that carry address and data information is dependent on the protocol and specific command. This table uses "X-X-X" format to specify the number of device pins used in transferring command, address and data information, for example:
command - address - data = 1-1-2 or 4-4-4, etc.

Table 31: **Command Definitions**

Command	Code	Command-Address-Data Pattern			Address Bytes	Dummy Clock Cycles			Data Bytes	Notes
		Standard SPI	DPI	QPI		Standard SPI	DPI	QPI		
Software RESET										
Reset Enable	66h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
Reset Memory	99h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
READ ID										
Read ID	9Eh/9Fh	1-0-1	— —	— —	0	0	— —	— —	1 to 20	— —
Multiple IO Read ID	AFh	1-0-1	2-0-2	4-0-4	0	0	0	0	1 to 20	— —
Read Serial Flash Discovery Parameter	5Ah	1-1-1	2-2-2	4-4-4	3	8	8	8	1 to ∞	1
READ MEMORY										
Read	03h	1-1-1	— —	— —	3(4)	0	— —	— —	1 to ∞	2
Fast Read	0Bh	1-1-1	2-2-2	4-4-4	3(4)	8	8	10	1 to ∞	2, 3
Dual Output Fast Read	3Bh	1-1-2	2-2-2	— —	3(4)	8	8	— —	1 to ∞	2, 3
Dual Input/Output Fast Read	BBh	1-2-2	2-2-2	— —	3(4)	8	8	— —	1 to ∞	2, 3
Quad Output Fast Read	6Bh	1-1-4	— —	4-4-4	3(4)	8	— —	10	1 to ∞	2, 3
Quad Input/Output Fast Read	EBh	1-4-4	— —	4-4-4	3(4)	10	— —	10	1 to ∞	2, 3
DTR Fast Read	0Dh	1-1-1	2-2-2	4-4-4	3(4)	6	6	8	1 to ∞	2, 3
DTR Dual Output Fast Read	3Dh	1-1-2	2-2-2	— —	3(4)	6	6	— —	1 to ∞	2, 3
DTR Dual Input/Output Fast Read	BDh	1-2-2	2-2-2	— —	3(4)	6	6	— —	1 to ∞	2, 3

DTR Quad Output Fast Read	6Dh	1-1-4	— —	4-4-4	3(4)	6	— —	8	1 to ∞	2, 3
DTR Quad Input/Output Fast Read	EDh	1-4-4	— —	4-4-4	3(4)	8	— —	8	1 to ∞	2, 3
Quad Input/Output Word Read	E7h	1-4-4	— —	4-4-4	3(4)	4	— —	4	1 to ∞	2
READ MEMORY with 4-Byte Address										
4-Byte Read	13h	1-1-1	— —	— —	4	0	— —	— —	1 to ∞	3
4-Byte Fast Read	0Ch	1-1-1	2-2-2	4-4-4	4	8	8	10	1 to ∞	3
4-Byte Dual Output Fast Read	3Ch	1-1-2	2-2-2	— —	4	8	8	— —	1 to ∞	3
4-Byte Dual Input/Output Fast Read	BCh	1-2-2	2-2-2	— —	4	8	8	— —	1 to ∞	3
4-Byte Quad Output Fast Read	6Ch	1-1-4	— —	4-4-4	4	8	— —	10	1 to ∞	3
4-Byte Quad Input/Output Fast Read	ECh	1-4-4	— —	4-4-4	4	10	— —	10	1 to ∞	3
4-Byte DTR Fast Read	0Eh	1-1-1	2-2-2	4-4-4	4	6	6	8	1 to ∞	3
4-Byte DTR Dual Input/Output Fast Read	BEh	1-2-2	2-2-2	— —	4	6	6	— —	1 to ∞	3
4-Byte DTR Quad Input/Output Fast Read	EEh	1-4-4	— —	4-4-4	4	8	— —	8	1 to ∞	3
WRITE Control										
Write Enable	06h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
Write Disable	04h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
READ REGISTER										
Read Status Register	05h	1-0-1	2-0-2	4-0-4	0	0	0	0	1 to ∞	— —
Read Flag Status Register	70h	1-0-1	2-0-2	4-0-4	0	0	0	0	1 to ∞	— —
Read Nonvolatile Configuration Register	B5h	1-0-1	2-0-2	4-0-4	0	0	0	0	2 to ∞	— —
Read Volatile Configuration Register	85h	1-0-1	2-0-2	4-0-4	0	0	0	0	1 to ∞	— —
Read Enhanced Volatile Configuration Register	65h	1-0-1	2-0-2	4-0-4	0	0	0	0	1 to ∞	— —
Read Extended Address Register	C8h	1-0-1	2-0-2	4-0-4	0	0	0	0	1 to ∞	— —
WRITE REGISTER										
Write Status Register	01h	1-0-1	2-0-2	4-0-4	0	0	0	0	1	4
Write Nonvolatile Configuration Register	B1h	1-0-1	2-0-2	4-0-4	0	0	0	0	2	4

Write Volatile Configuration Register	81h	1-0-1	2-0-2	4-0-4	0	0	0	0	1	4
Write Enhanced Volatile Configuration Register	61h	1-0-1	2-0-2	4-0-4	0	0	0	0	1	4
Write Extended Address Register	C5h	1-0-1	2-0-2	4-0-4	0	0	0	0	1	4
CLEAR FLAG STATUS REGISTER										
Clear Flag Status Register	50h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
PROGRAM										
Page Program	02h	1-1-1	2-2-2	4-4-4	3(4)	0	0	0	1 to 256	4
Dual Input Fast Program	A2h	1-1-2	2-2-2	— —	3(4)	0	0	— —	1 to 256	2, 4
Extended Dual Input Fast Program	D2h	1-2-2	2-2-2	— —	3(4)	0	0	— —	1 to 256	2, 4
Quad Input Fast Program	32h	1-1-4	— —	4-4-4	3(4)	0	— —	0	1 to 256	2, 4
Extended Quad Input Fast Program	38h	1-4-4	— —	4-4-4	3(4)	0	— —	0	1 to 256	2, 4
PROGRAM with 4-Byte Address										
4-Byte Page Program	12h	1-1-1	2-2-2	4-4-4	4	0	0	0	1 to 256	4
4-Byte Quad Input Fast Program	34h	1-1-4	— —	4-4-4	4	0	— —	0	1 to 256	4
4-Byte Quad Input Extended Fast Program	3Eh	1-4-4	— —	4-4-4	4	0	— —	0	1 to 256	4
ERASE										
32KB Subsector Erase	52h	1-1-0	2-2-0	4-4-0	3(4)	0	0	0	0	2, 4
4KB Subsector Erase	20h	1-1-0	2-2-0	4-4-0	3(4)	0	0	0	0	2, 4
64KB Sector Erase	D8h	1-1-0	2-2-0	4-4-0	3(4)	0	0	0	0	2, 4
Bulk Erase	C7h/60h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	4
ERASE with 4-Byte Address										
4-Byte Sector Erase	DCh	1-1-0	2-2-0	4-4-0	4	0	0	0	0	4
4-Byte 4KB Subsector Erase	21h	1-1-0	2-2-0	4-4-0	4	0	0	0	0	4
4-Byte 32KB Subsector Erase	5Ch	1-1-0	2-2-0	4-4-0	4	0	0	0	0	4
SUSPEND/RESUME										
Program/Erase Suspend	75h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —

Program/Erase Resume	7Ah	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
OTP Operations										
Read OTP Array	4Bh	1-1-1	2-2-2	4-4-4	3(4)	8	8	10	1 to 64	2, 3
Program OTP Array	42h	1-1-1	2-2-2	4-4-4	3(4)	0	0	0	1 to 64	2, 4
4-BYTE ADDRESS MODE										
Enter 4-Byte Address Mode	B7h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
Exit 4-Byte Address Mode	E9h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
QPI PROTOCOL										
Enter Quad Input/Output Mode	35h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
Reset Quad Input/Output Mode	F5h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
Deep Power-Down										
Enter Deep Power Down	B9h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
Release From Deep Power Down	ABh	1-0-0	2-0-0	4-0-0	0	0	0	0	0	— —
ADVANCED SECTOR PROTECTION										
Read Sector Protection	2Dh	1-0-1	2-0-2	4-0-4	0	0	0	0	1 to ∞	— —
Program Sector Protection	2Ch	1-0-1	2-0-2	4-0-4	0	0	0	0	2	4
Read Volatile Lock Bits	E8h	1-1-1	2-2-2	4-4-4	3(4)	0	0	0	1 to ∞	2
Write Volatile Lock Bits	E5h	1-1-1	2-2-2	4-4-4	3(4)	0	0	0	1	2, 4
Read Nonvolatile Lock Bits	E2h	1-1-1	2-2-2	4-4-4	4	0	0	0	1 to ∞	— —
Write Nonvolatile Lock Bits	E3h	1-1-0	2-2-0	4-4-0	4	0	0	0	0	4
Erase Nonvolatile Lock Bits	E4h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	4
Read Global Freeze Bit	A7h	1-0-1	— —	— —	0	0	0	0	1 to ∞	— —
Write Global Freeze Bit	A6h	1-0-0	2-0-0	4-0-0	0	0	0	0	0	4
Read Password	27h	1-0-1	— —	— —	0	0	0	0	1 to ∞	— —
Write Password	28h	1-0-1	2-0-2	4-0-4	0	0	0	0	8	4
Unlock Password	29h	1-0-1	2-0-2	4-0-4	0	0	0	0	8	— —
ADVANCED SECTOR PROTECTION with 4-Byte Address										

4-Byte Read Volatile Lock Bits	E0h	1-1-1	2-2-2	4-4-4	4	0	0	0	1 to ∞	——
4-Byte Write Volatile Lock Bits	E1h	1-1-1	2-2-2	4-4-4	4	0	0	0	1	4

Notes:

1. The Read Serial Flash Discovery Parameter command only accepts 3-byte address no matter whether the device is in 3-byte or 4-byte address mode.
2. Commands with "Address Bytes" column being "3(4)" require 3 or 4 bytes of address if the device is in 3-byte address mode or 4-byte address mode, respectively.
3. The number of dummy clock cycles is selectable via nonvolatile and volatile configuration registers.
4. The Write Enable command is required before these operations.

10.2. Software Reset Operations

10.2.1. Reset Enable (66h) and Reset Memory (99h)

The Reset commands aborts all on-going internal operations, and brings the device back to its default power-on state. All volatile settings are lost, including:

WEL, WIP;
Flag Status Register;
Extended Address Regiseter;
Volatile Configuration Register;
Enhanced Volatile Configuration Register.

To perform software reset operation on the device, the command sequence is as follows:

Drive CS# low --> Send in 66h command byte --> Drive CS# high --> A minimum time duration of tSHSL2 is required --> Drive CS# low --> Send in 99h command byte --> Drive CS# high --> A minimum time duration of tSHSL3 is required --> The device is ready to accept upcoming commands.

Data corruption may occur if Reset command is used to interrupt an ongoing or suspended Write, Program or Erase operation. To prevent this, it is recommended to check WIP, SUS2 and SUS1 bits before issuing this command.

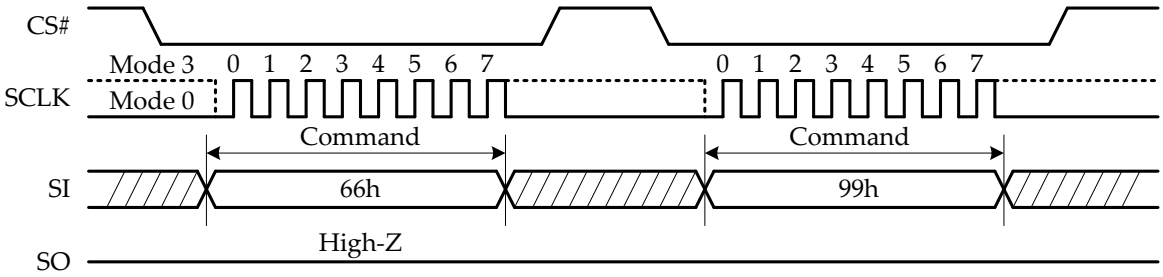


Figure 10: **Reset Enable (66h) and Reset Memory (99h) Command Sequence**

The above timing diagram presents the 66h and 99h commands in standard SPI protocol. Other protocols are also supported:

For DPI protocol, the command bytes are communicated on IO0 and IO1 pins;

for QPI protocol, the command bytes are communicated on IO0, IO1, IO2 and IO3 pins;

for standard SPI protocol in DTR mode, the command bytes are transferred on SI pin on both edges of SCLK;

for DPI protocol in DTR mode, the command bytes are transferred on IO0 and IO1 pins on both edges of SCLK;

for QPI protocol in DTR mode, the command bytes are transferred on IO0, IO1, IO2 and IO3 pins on both edges of SCLK.

10.3. Read ID Operations

10.3.1. Read ID (9Eh/9Fh) and Multiple IO Read ID (AFh)

These commands output device ID information. For ID definitions, see Section *6.1 Identification*. An RDID command during Write, Program or Erase cycle is ignored.

The command sequence is:

Drive CS# pin low --> Shift in 9Eh/9Fh/AFh command byte --> Shift out ID bytes on one, two or four pins --> The host may terminate the command by driving CS# high at any time during data output.

As long as CS# keeps low, the three IDs will be repetitively output in turns.

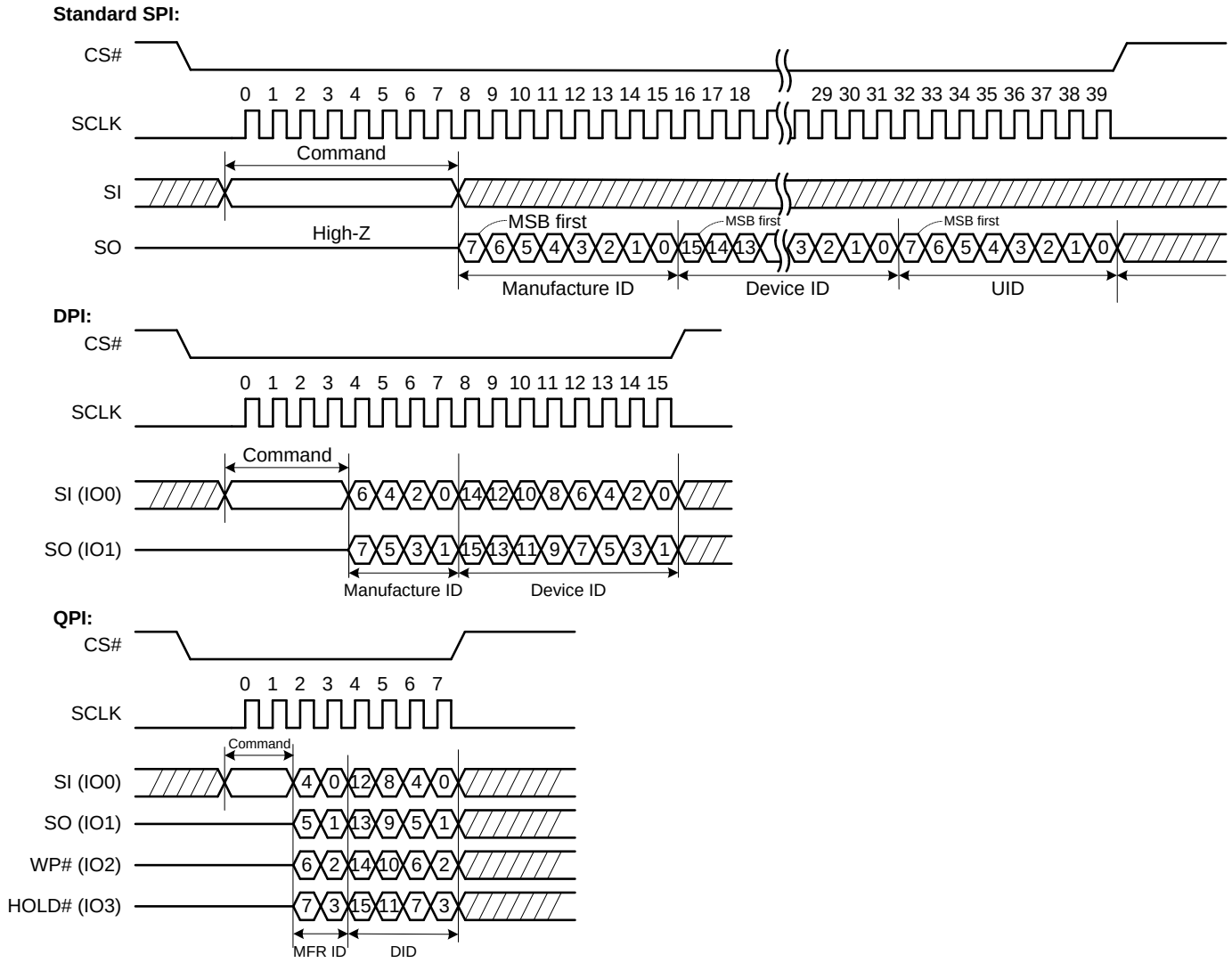


Figure 11: **Read ID (9Eh/9Fh) and Multiple IO Read ID (AFh)**

10.3.2. Read Serial Flash Discovery Parameter (5Ah)

The SFDP information is stored in a standard set of tables, which contain the functional and feature capabilities of the device. These tables can be interrogated by the host to make adjustments needed to accommodate to different features of devices from various vendors. SFDP is a JEDEC Standard (JESD216).

The details of SFDP tables are specified in Section 0 *Notes:*

5. The address bits "X" are don't care.

SFDP Register.

The 5Ah command sequence is:

Drive CS# low --> Shift in 5Ah command byte on SI --> Shift in three address bytes --> Shift in eight dummy clock cycles --> Shift out SFDP information starting from the specified address --> The host may terminate the command by driving CS# high at any time during data output.

Even if the device is in 4-byte address mode, this command always uses 3-byte address. After output data reaches the 2048-byte boundary, it wraps back and continues data output from address 0.

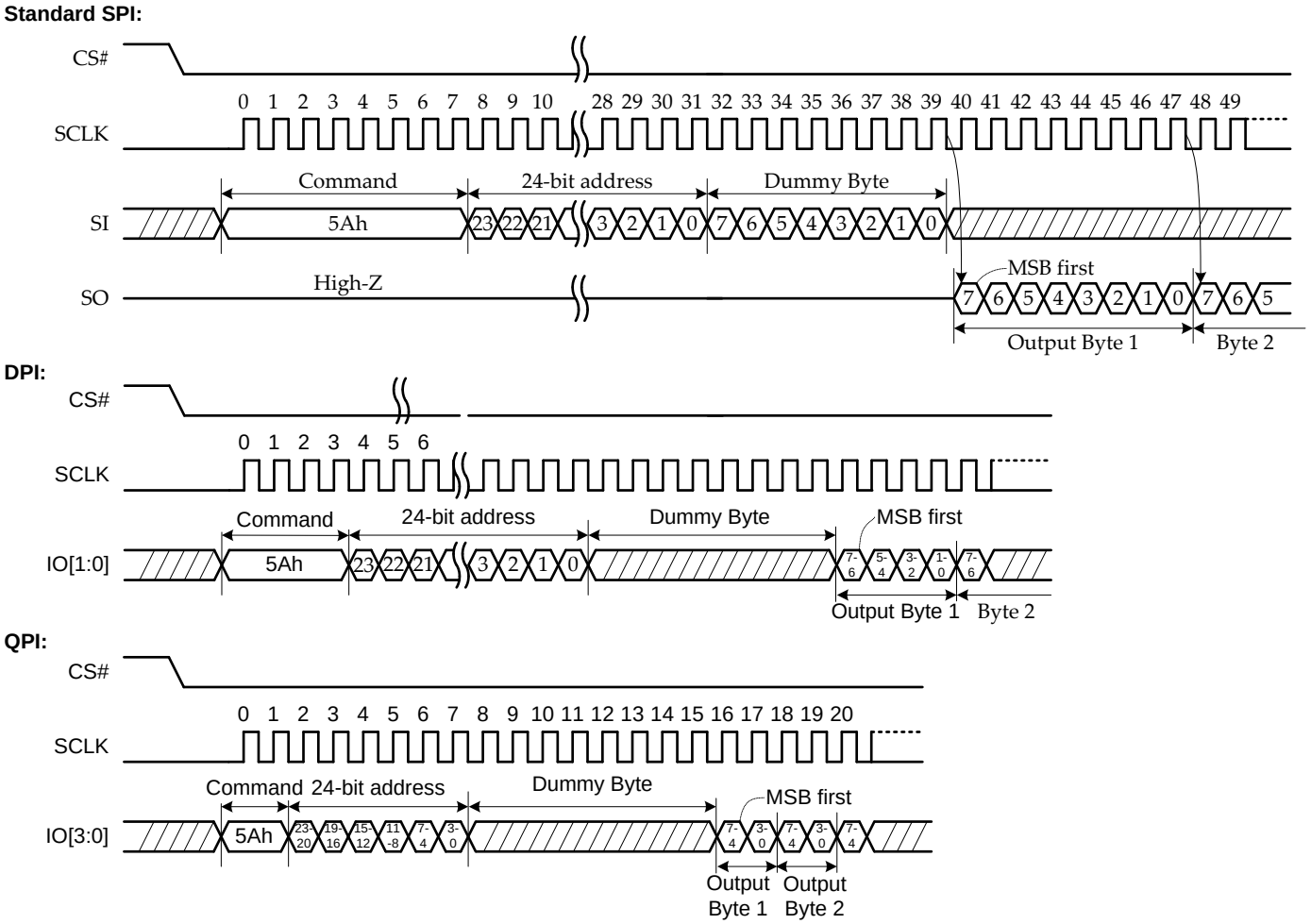


Figure 12: **Read Serial Flash Discovery Parameter (5Ah) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).
2. For DPI protocol, C_X=3+$\frac{(A[MAX]+1)}{2}$.
3. For QPI protocol, C_X=1+$\frac{(A[MAX]+1)}{4}$.

10.4. Read Memory Operations

To perform read operation, the command sequence is as folows:

Drive CS# low --> Shift in command byte --> Shift in address bytes --> Shift out read data starting from the specified address --> The host may terminate the command by driving CS# high at any time during data output.

Depending on the address mode, read commands may require a 3-byte address (A23~A0) or 4-byte address (A31-A0). The address can point to any byte location in the main memory array. After each byte is shifted out, the address automatically increments to the next byte location; therefore, the entire memory can be output with a single READ command. After output data reaches the boundary, the output will roll back and continue to shift out data from the beginning address.

The command is rejected if a Write, Program or Erase operation is in progress.

DTR commands will follow DTR protocol regardless of the DTRB setting in registers, while other commands work in DTR mode only when DTRB bit is enabled; similarly, 4-Byte commands use 4 bytes of address regardless of register settings, while other commands work in 4-byte address mode only when ADP bit is set accordingly.

Compared with other read commands, Fast Read commands support higher frequency fc.

E7h command's lowest address bit A0 must be 0, and only four dummy clocks are needed; this command supports standard SPI and QPI, but does not support DPI or DTR protocols.

10.4.1. Read (03h/13h)

Standard SPI:

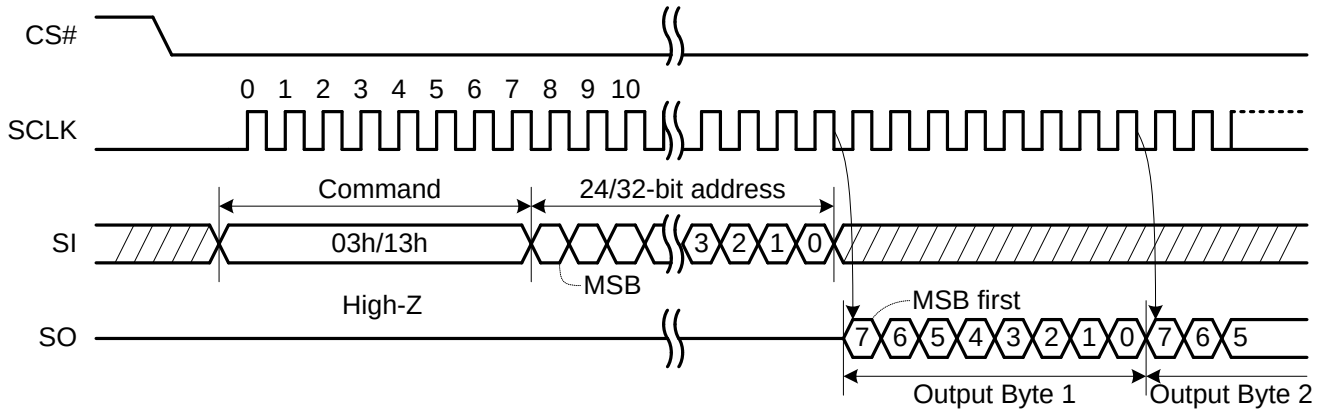


Figure 13: **Read (03h/13h) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).
2. For DPI protocol, C_X=3+$\frac{(A[MAX]+1)}{2}$.
3. For QPI protocol, C_X=1+$\frac{(A[MAX]+1)}{4}$.
4. 03h supports both 3-Byte and 4-Byte address modes.
5. 13h supports only 4-Byte address mode.

10.4.2. Fast Read (0Bh/0Ch)

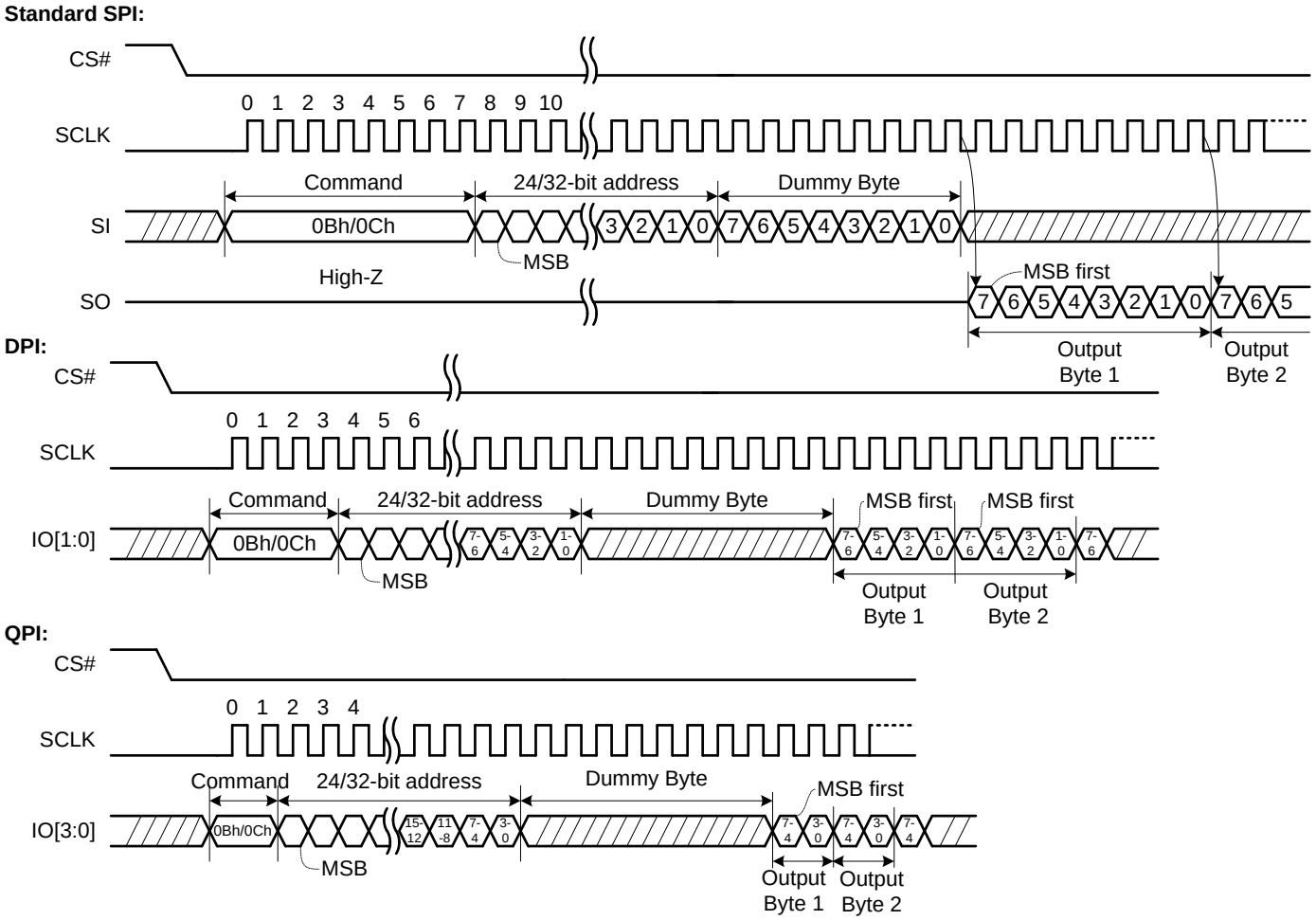


Figure 14: **Fast Read (0Bh/0Ch) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).
2. For DPI protocol, C_X=3+$\frac{(A[MAX]+1)}{2}$.
3. For QPI protocol, C_X=1+$\frac{(A[MAX]+1)}{4}$.
4. 0Bh supports both 3-Byte and 4-Byte address modes.
5. 0Ch supports only 4-Byte address mode.

10.4.3. Dual Output Fast Read (3Bh/3Ch)

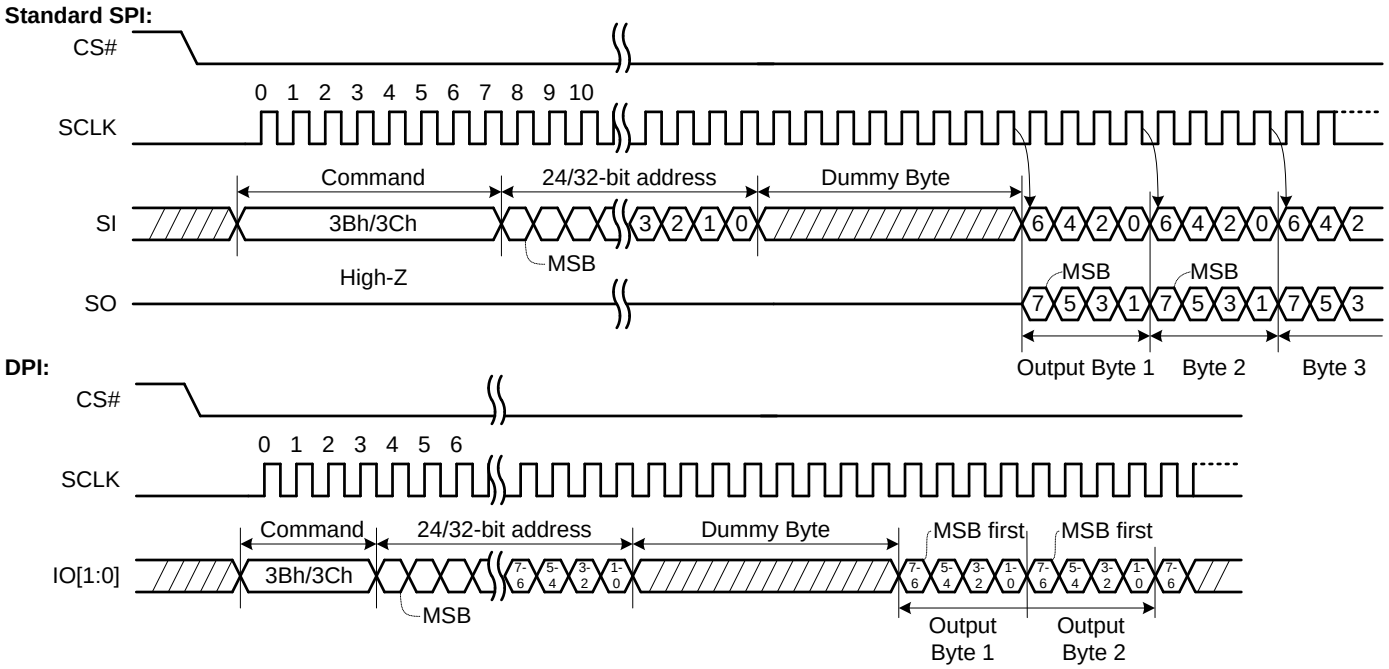


Figure 15: **Dual Output Fast Read (3Bh/3Ch) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).
2. For DPI protocol, C_X=3+$\frac{(A[MAX]+1)}{2}$.
3. 3Bh supports both 3-Byte and 4-Byte address modes.
4. 3Ch supports only 4-Byte address mode.

10.4.4. Dual Input/Output Fast Read (BBh/BCh)

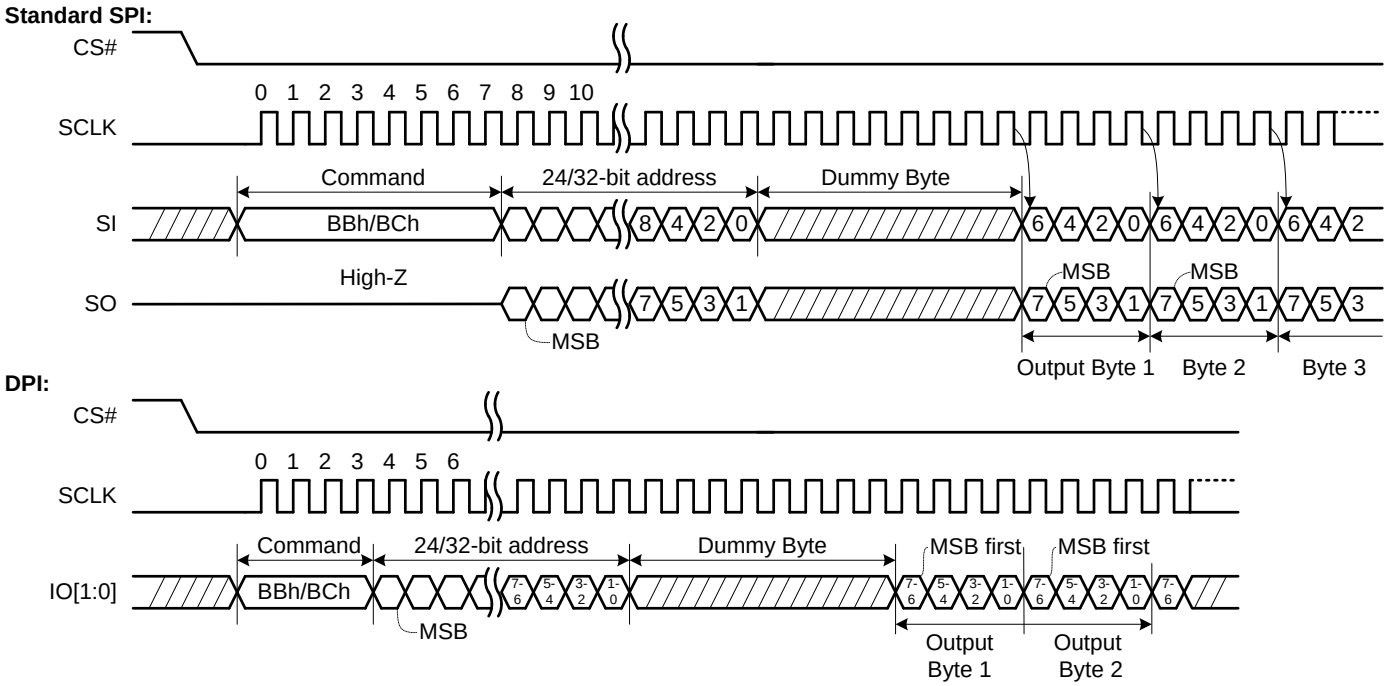


Figure 16: **Dual Input/Output Fast Read (BBh/BCh) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).

2. For DPI protocol, $C_X=3+\frac{(A[MAX]+1)}{2}$.
3. BBh supports both 3-Byte and 4-Byte address modes.
4. BCh supports only 4-Byte address mode.

10.4.5. Quad Output Fast Read (6Bh/6Ch)

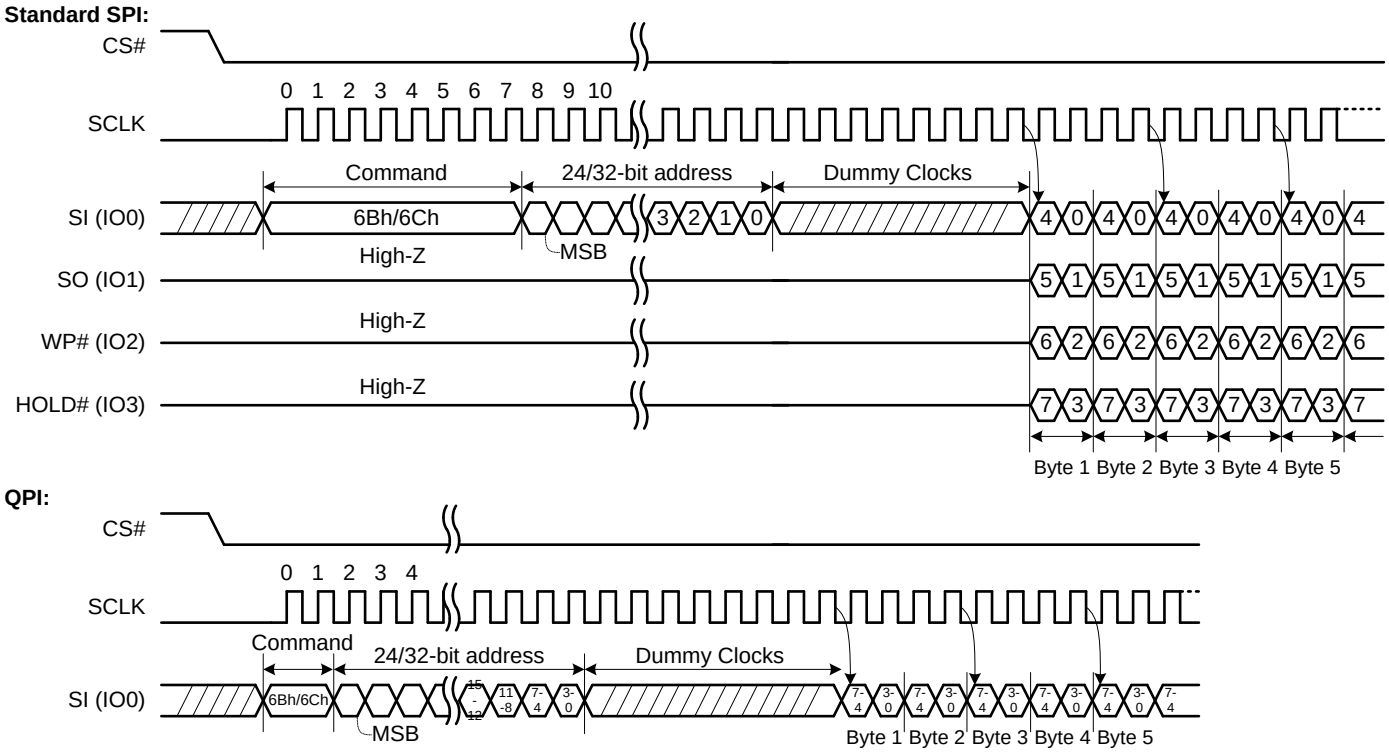


Figure 17: **Quad Output Fast Read (6Bh/6Ch) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+(A[MAX]+1)$.
2. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{4}$.
3. 6Bh supports both 3-Byte and 4-Byte address modes.
4. 6Ch supports only 4-Byte address mode.

10.4.6. Quad Input/Output Fast Read (EBh/ECh)

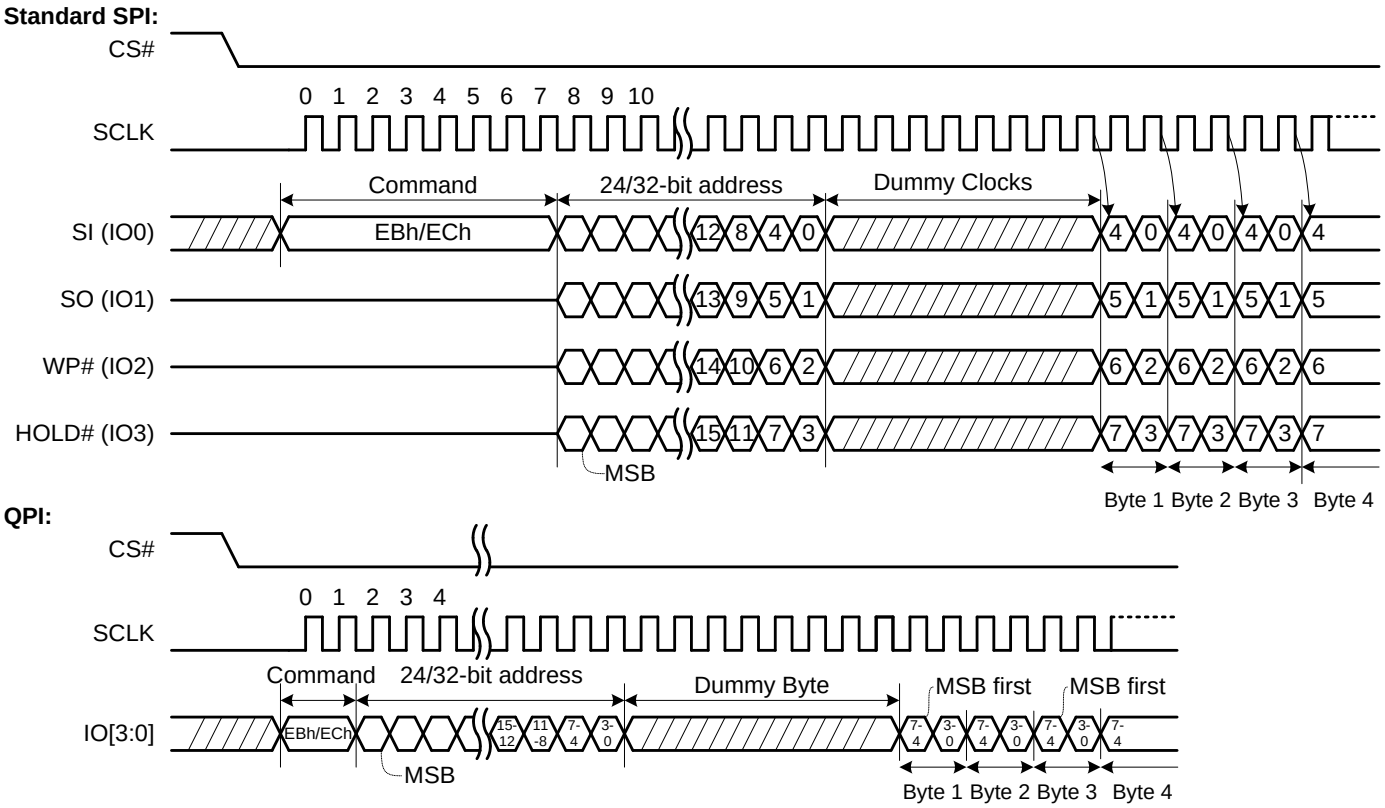


Figure 18: **Quad Input/Output Fast Read (EBh/ECh) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{4}$.
2. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{4}$.
3. EBh supports both 3-Byte and 4-Byte address modes.
4. ECh supports only 4-Byte address mode.

10.4.7. Quad Input/Output Word Read (E7h)

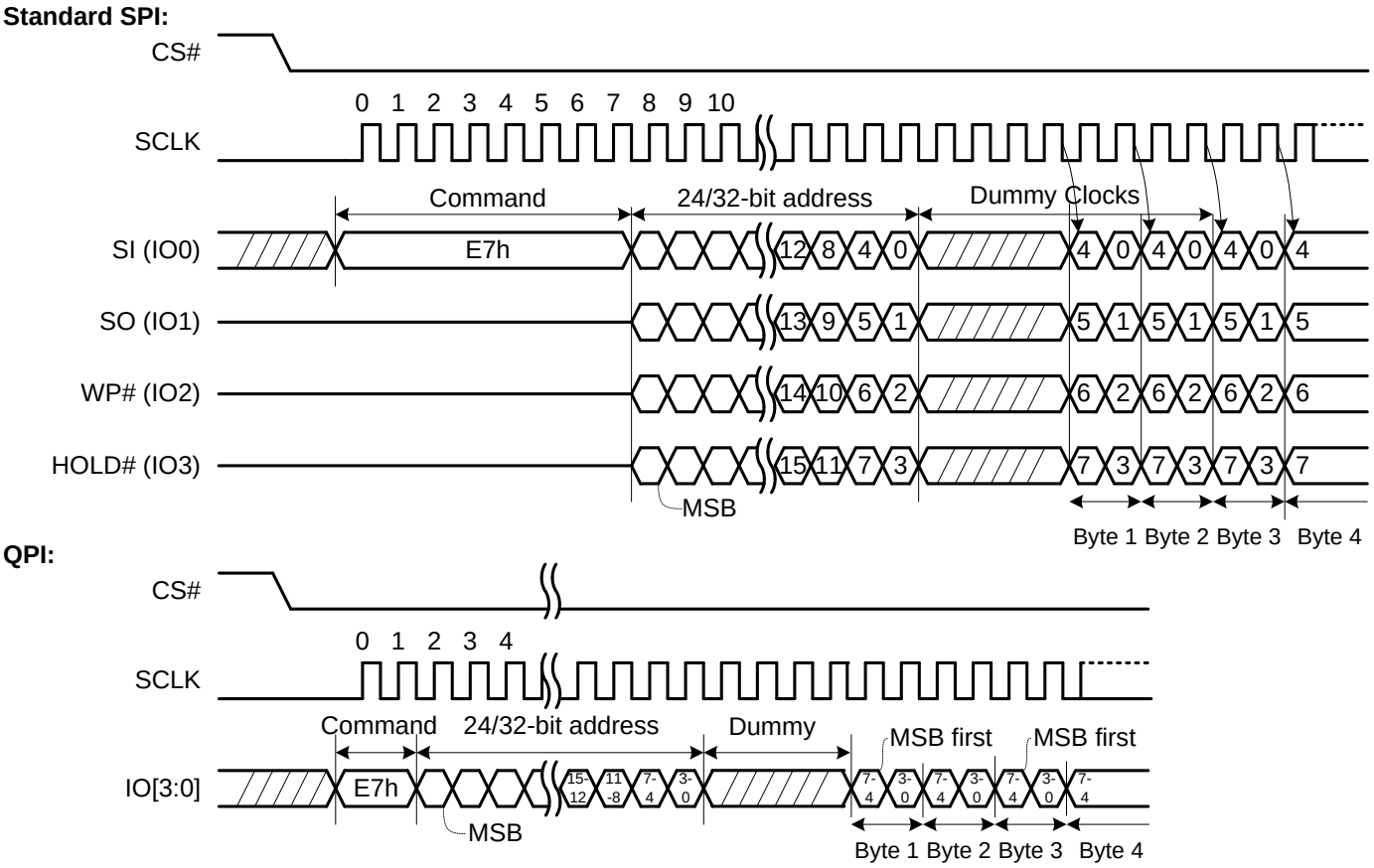


Figure 19: **Quad Input/Output Word Read (E7h) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{4}$.
2. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{4}$.
3. E7h supports both 3-Byte and 4-Byte address modes.

10.4.8. DTR Fast Read (0Dh/0Eh)

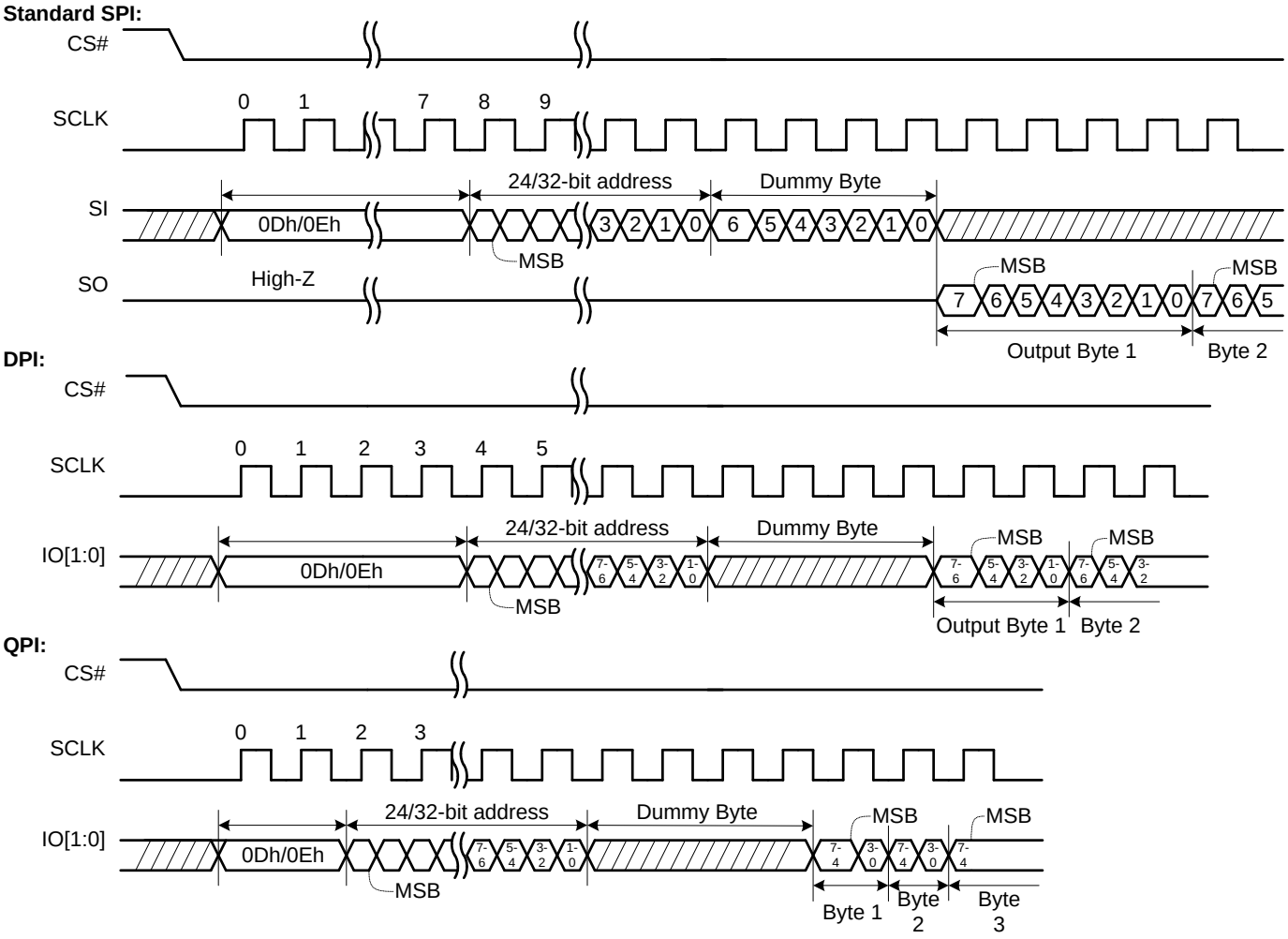


Figure 20: **DTR Fast Read (0Dh/0Eh) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{2}$.
2. For DPI protocol, $C_X=3+\frac{(A[MAX]+1)}{4}$.
3. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{8}$.
3. 0Dh supports both 3-Byte and 4-Byte address modes.
4. 0Eh supports only 4-Byte address mode.

10.4.9. DTR Dual Output Fast Read (3Dh)

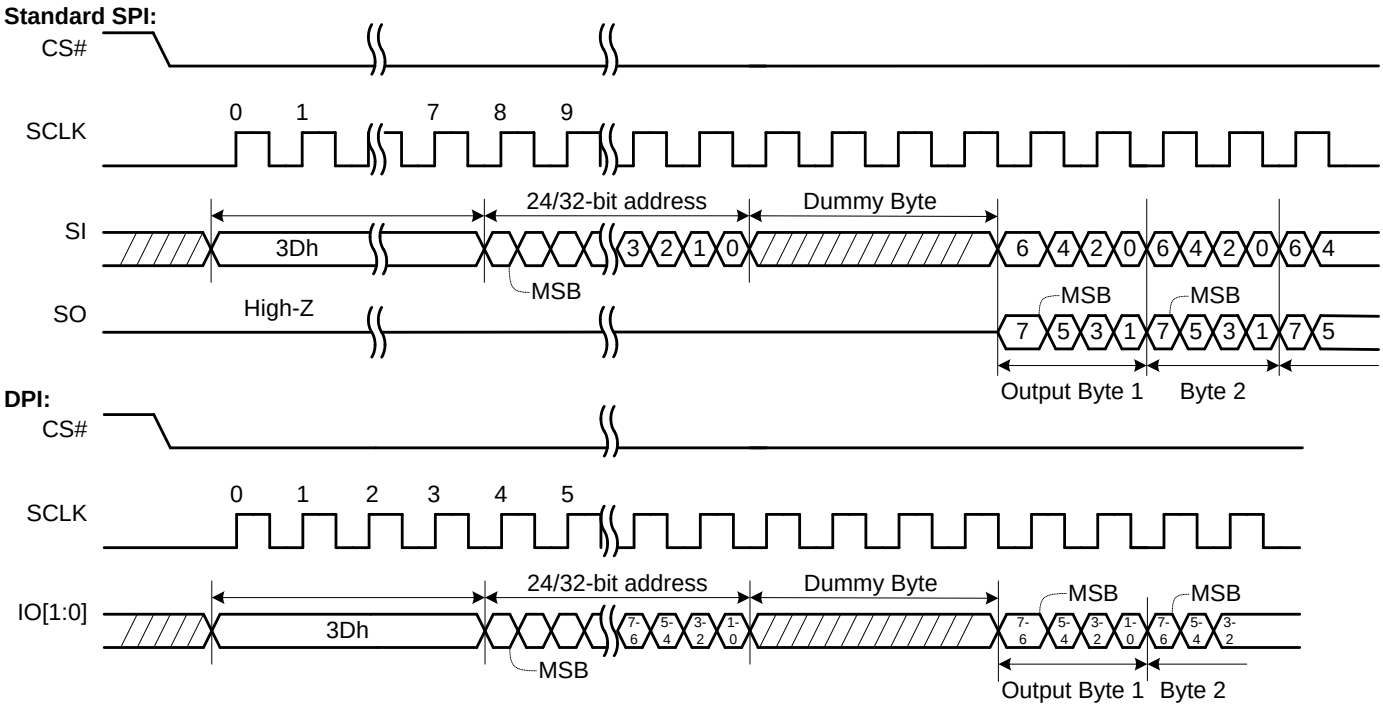


Figure 21: **DTR Dual Output Fast Read (3Dh) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{2}$.
2. For DPI protocol, $C_X=3+\frac{(A[MAX]+1)}{4}$.
3. 3Dh supports both 3-Byte and 4-Byte address modes.

10.4.10. DTR Dual Input/Output Fast Read (BDh/BEh)

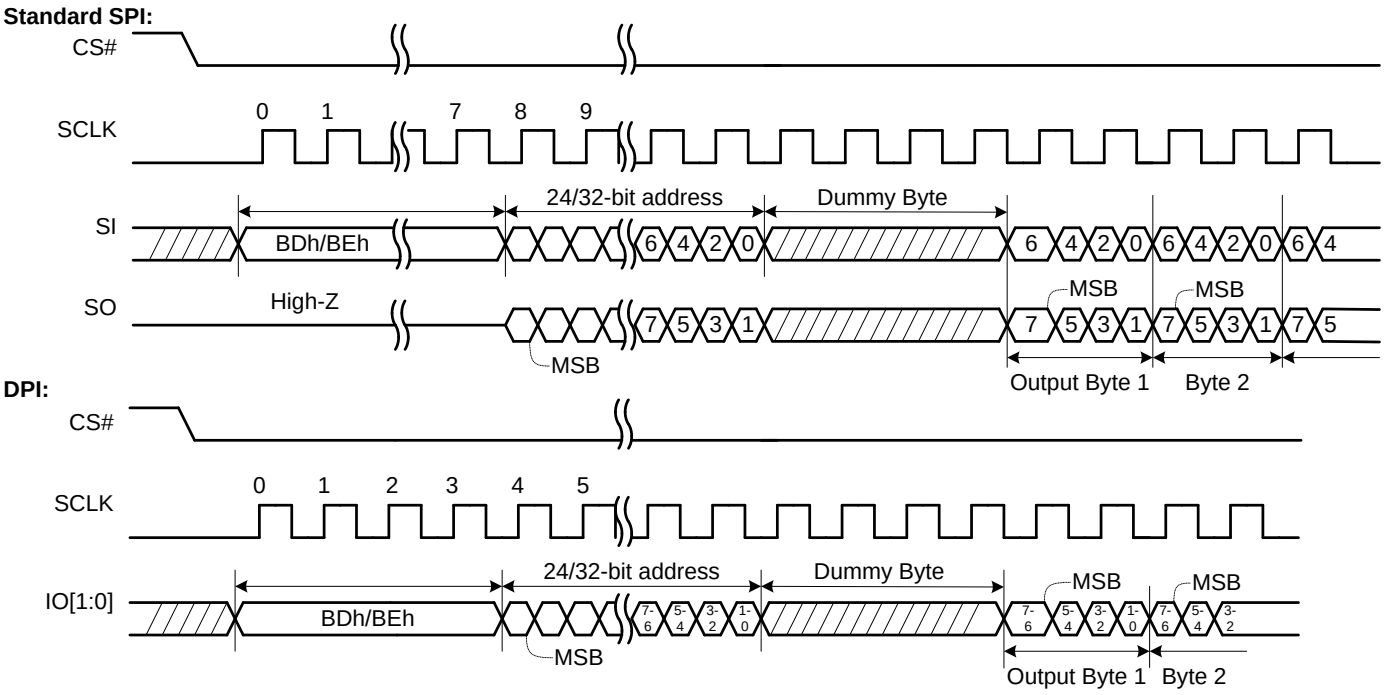


Figure 22: **DTR Dual Input/Output Fast Read (BDh/BEh) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{4}$.
2. For DPI protocol, $C_X=3+\frac{(A[MAX]+1)}{8}$.
3. BDh supports both 3-Byte and 4-Byte address modes.
4. BEh supports only 4-Byte address mode.

10.4.11. DTR Quad Output Fast Read (6Dh)

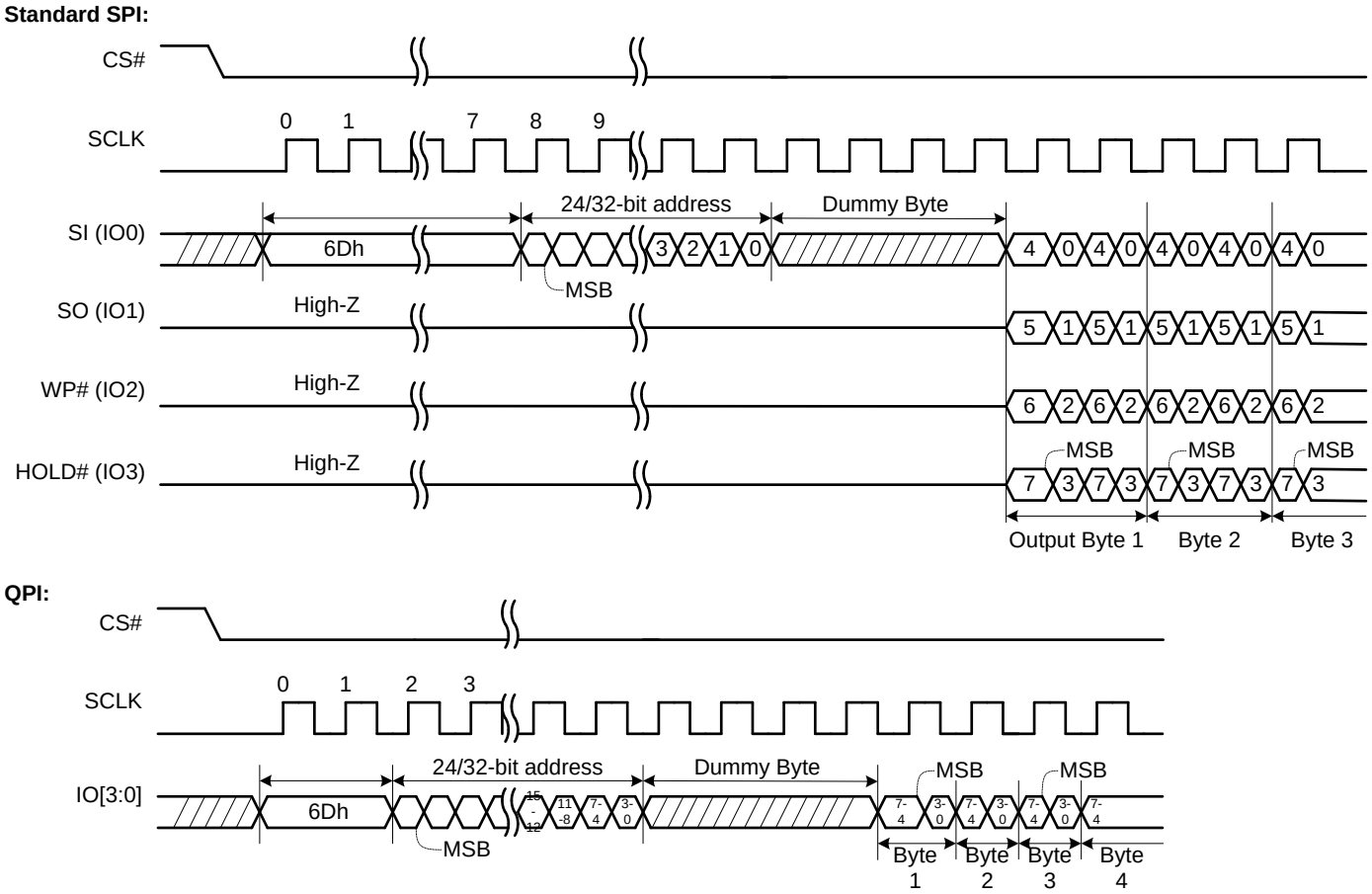


Figure 23: **DTR Quad Output Fast Read (6Dh) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{2}$.
2. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{8}$.
3. 6Dh supports both 3-Byte and 4-Byte address modes.

10.4.12. DTR Quad Input/Output Fast Read (EDh/EEh)

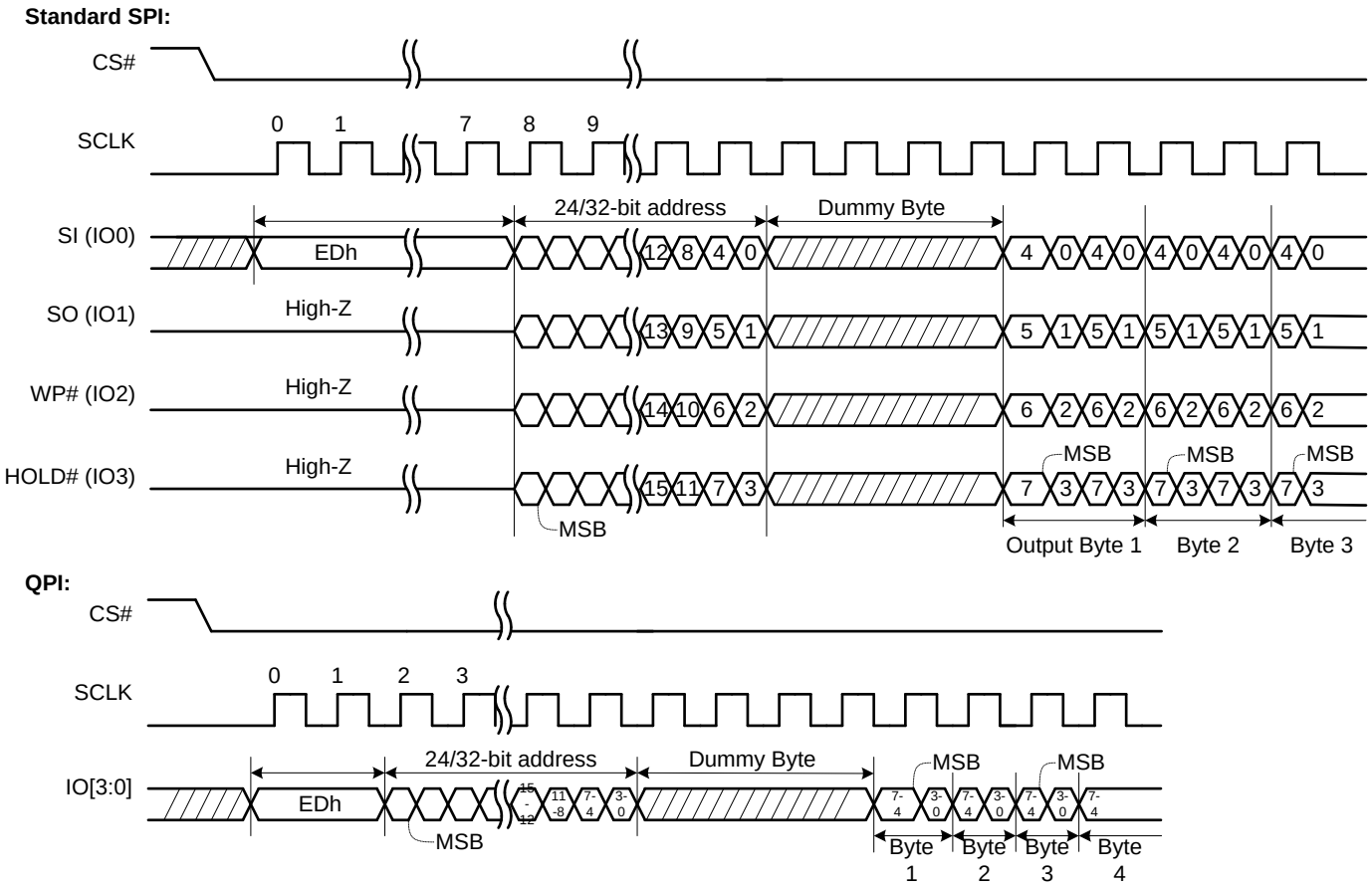


Figure 24: **DTR Quad Input/Output Fast Read (EDh/EEh) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{8}$.
2. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{8}$.
3. EDh supports both 3-Byte and 4-Byte address modes.
4. EEh supports only 4-Byte address mode.

10.5. Write Operations

10.5.1. Write Enable (WREN) (06h)

The WREN command sets the WEL bit to 1, which is a prerequisite prior to every Program, Erase and Write command, as is specified in ***Table 31:*** *Command Definitions*; these commands are ignored by the device without prior WREN command.

The command sequence is:

Drive CS# low --> Send 06h command --> Drive CS# high.

The CS# pin should be driven High after the command byte is input to the device, otherwise the command is not executed.

For standard SPI mode, the command byte is transferred on SI.

For DPI protocol, the command byte is communicated on IO0 and IO1 pins.

For QPI protocol, the command byte is communicated on IO0, IO1, IO2 and IO3 pins.

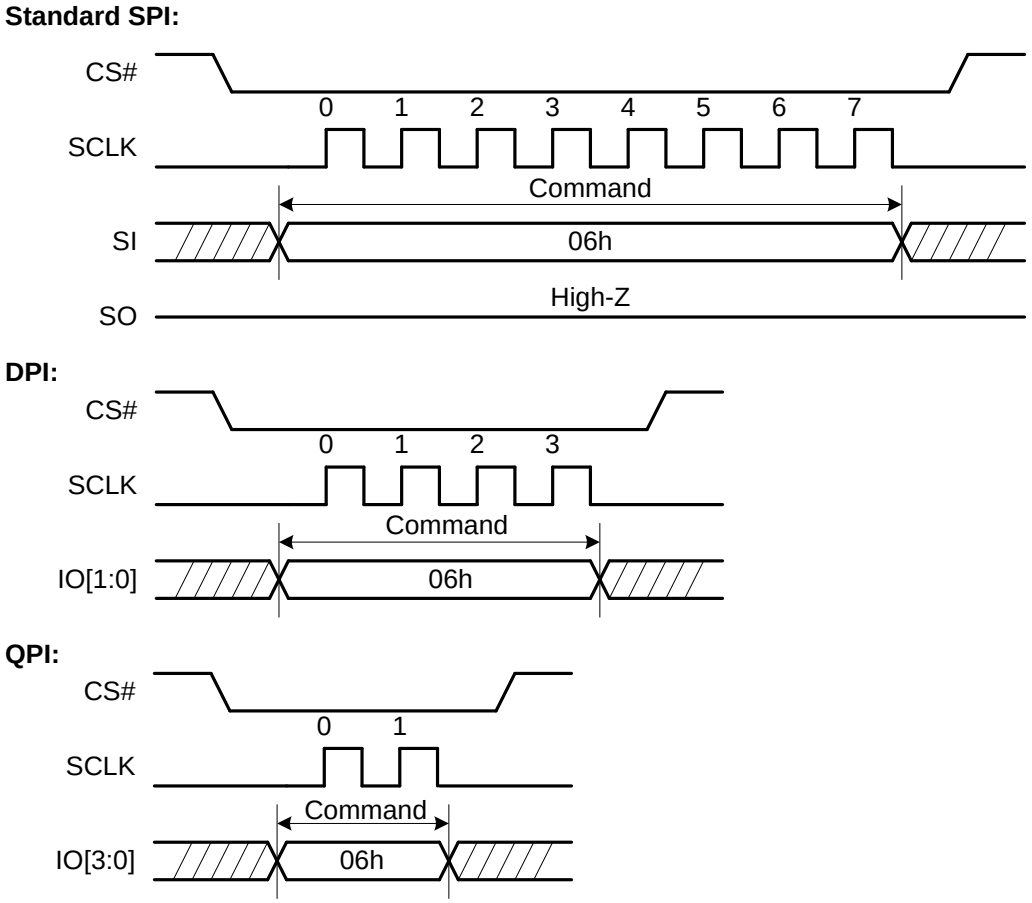


Figure 25: **Write Enable (WREN) (06h) Command Sequence**

10.5.2. Write Disable (WRDI) (04h)

The WRDI command clears the WEL bit to 0.

If protection error occurs, WRDI cannot clear the WEL bit; rather, a Clear Flag Status Register command can be used to clear WEL and PTE bits.

The command sequence is as follows:

Drive CS# low --> Send 04h command --> Drive CS# high.

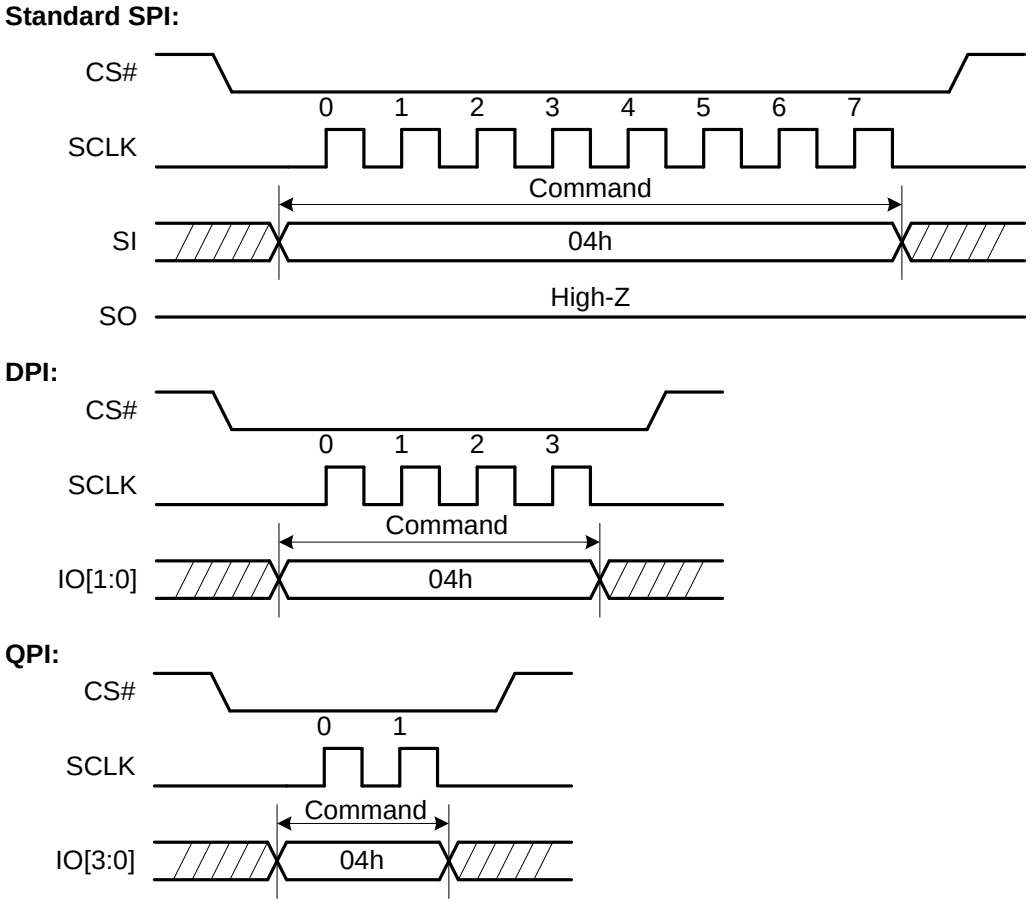


Figure 26: **Write Disable (WRDI) (04h) Command Sequence**

10.6. Read Register Operations

The 05h and 70h commands can be issued anytime, even while a Write, Program or Erase operation is in progress; actually, after one such operation, it is recommended to check the WIP or P/E controller bits before the next command is issued to the device.

For B5h command, data is output with low byte being the first byte, and high bit being the first bit. Reserved bits are 0 in output data.

For 85h, 65h and C8h commands, the same data byte is repeatedly output if the register is continuously read.

The command sequence is as follows:

Drive CS# low --> Send command byte --> Receive output data --> Drive CS# high.

10.6.1. Read Register (05h/70h/B5h/85h/65h/C8h)

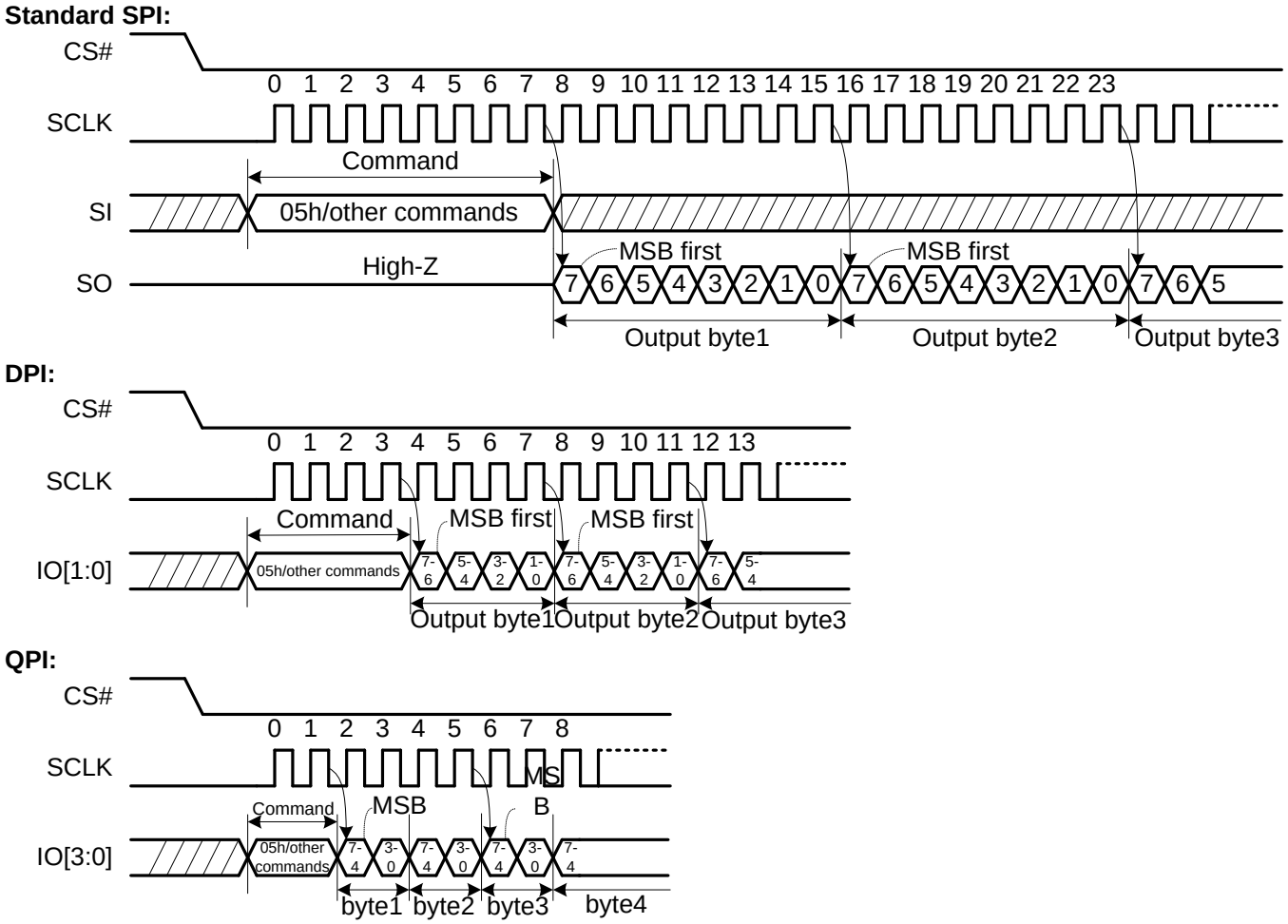


Figure 27: **Read Register (05h/70h/B5h/85h/65h/C8h) Command Sequence**

10.7. Write Register Operations

The Write Register commands change the values of various registers. Before issuing such a command, a WREN 06h command is needed to set the WEL bit.

The command sequence is as follows:

Drive CS# low --> Send command byte --> Send write data --> Drive CS# high.

The CS# pin should be driven High after the last bit of write data is input to the device, otherwise the command is not executed and WEL bit remains 1.

After CS# is driven high, a duration of tW or tNVCR is required before self-timed write cycle is complete. During tW or tNVCR, the host may poll the Status Register and Flag Status Register to detect the status of the operation; upon operation completion, the WIP bit is always cleared to 0 even if the Write operation fails.

For B1h command, input data starts from LSB.

10.7.1. Write Register (01h/B1h/81h/61h/C5h)

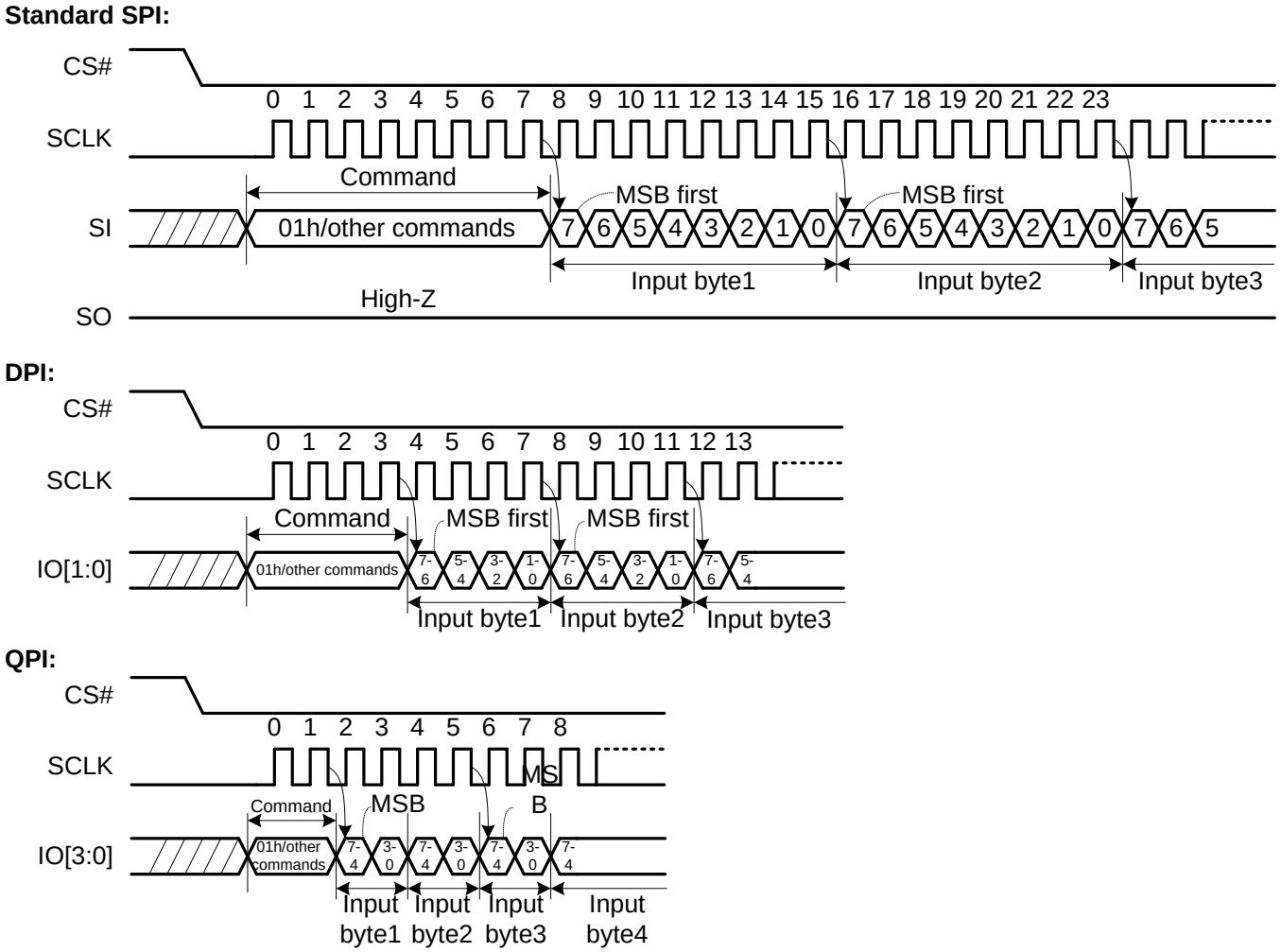


Figure 28: **Write Register (01h/B1h/81h/61h/C5h) Command Sequence**

Notes:

1. This timing diagram applies to all Write Register commands except Write Lock Register.
2. For Write Nonvolatile Configuration Register B1h command, input is two bytes and should start from LSB.

10.8. Clear Flag Status Register (50h)

This command clears the error bits (EE, PE, PTE) of Flag Status Register to all 0s.

The command sequence is as follows:

Drive CS# low --> Send command byte --> Drive CS# high.

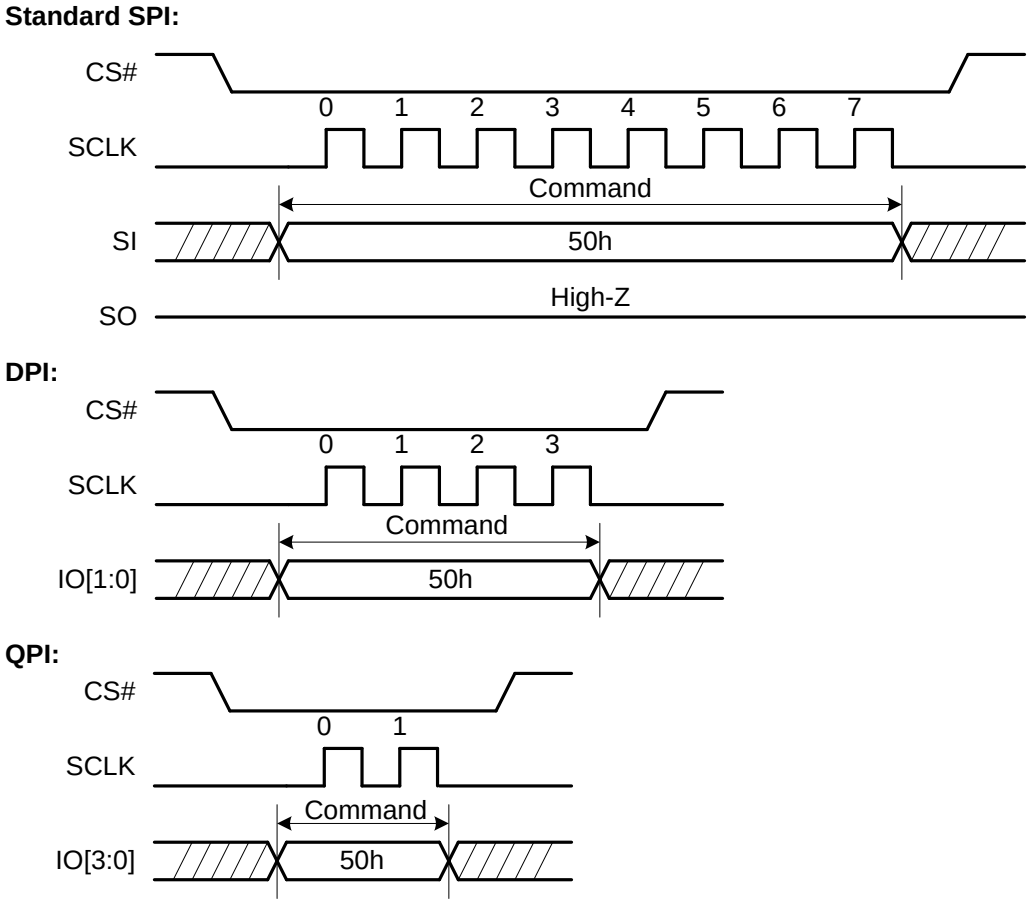


Figure 29: **Clear Flag Status Register (50h) Command Sequence**

10.9. Program Operations

A Program operation programs data to a specified location in the main memory array, which changes one or more data bits from 1 to 0, but not the reverse. To change data bits from 0 to 1, erase operation is required instead.

Before a Program operation, the WEL bit must be set to enable the device for programming operation. Attempting to program a memory location that has previously been programmed but not erased may corrupt the data.

The command sequence is as follows:

Drive CS# low --> Send command byte --> Send address bytes --> Send in data --> Drive CS# high.

The maximum amount of data to program in one operation is 256 bytes. The address specified in the Program command is the starting address of the program operation; this address can point to any location in the main memory array. The host may send in an arbitrary amount of data, however when the address points to the ending boundary of the current page, it automatically rolls back to the starting boundary of that page. Thus, all data bytes of a PP command fall within a single 256-byte page in the main array.

If more than 256 bytes of data are sent to the device, only the last 256 bytes take effect, and all previously latched data are discarded. If less than 256 data bytes are sent, they can be correctly programmed at the target addresses without affecting other bytes in the same page.

After CS# is driven high, a self-timed program cycle (t_{PP}) is initiated. While the program cycle is in progress, the WIP bit becomes 1, and WEL bit will be reset to 0 even if the program operation fails. It is recommended to continuously check the Status Register and Flag Status Register for the status of the operation. After the programming cycle is complete, the WEL bit is reset to 0.

The CS# pin must be driven high exactly at a byte boundary, otherwise the command is ignored. If CS# remains low after all program data is input, then the program operation is not executed, WEL remains 1, and error bits

are not set.

If a Program command is applied to a protected page, then it is not executed, WEL bit remains 1, and PTE and PE error bits are set.

DTR commands will follow DTR protocol regardless of the DTRB setting in registers, while other commands work in DTR mode only when DTRB bit is enabled; similarly, 4-Byte commands use 4 bytes of address regardless of register settings, while other commands work in 4-byte address mode only when ADP bit is set accordingly.

10.9.1. Page Program (PP) (02h/12h)

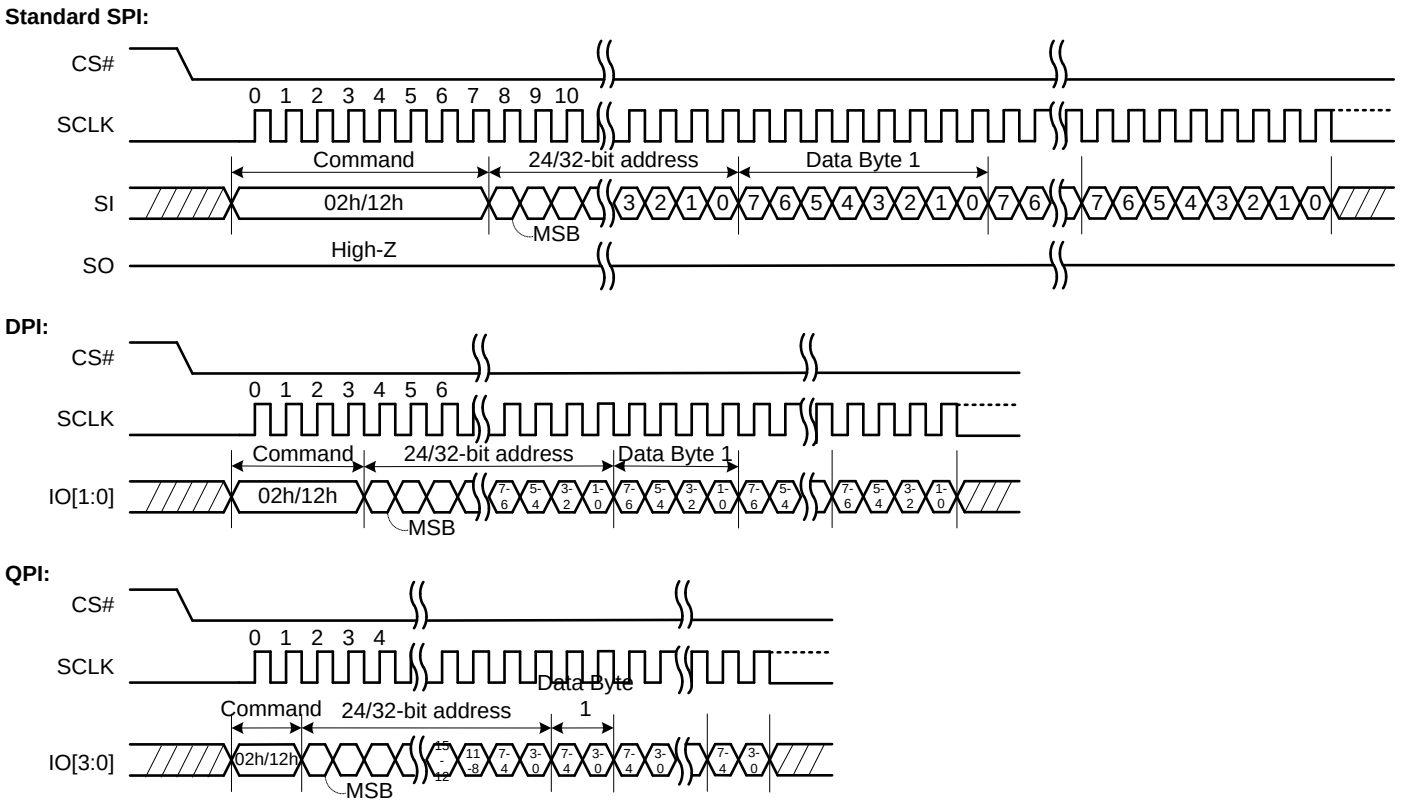


Figure 30: **Page Program (02h/12h) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).
2. For DPI protocol, C_X=3+$\frac{(A[MAX]+1)}{2}$.
3. For QPI protocol, C_X=1+$\frac{(A[MAX]+1)}{4}$.

10.9.2. Dual Input Fast Program (A2h)

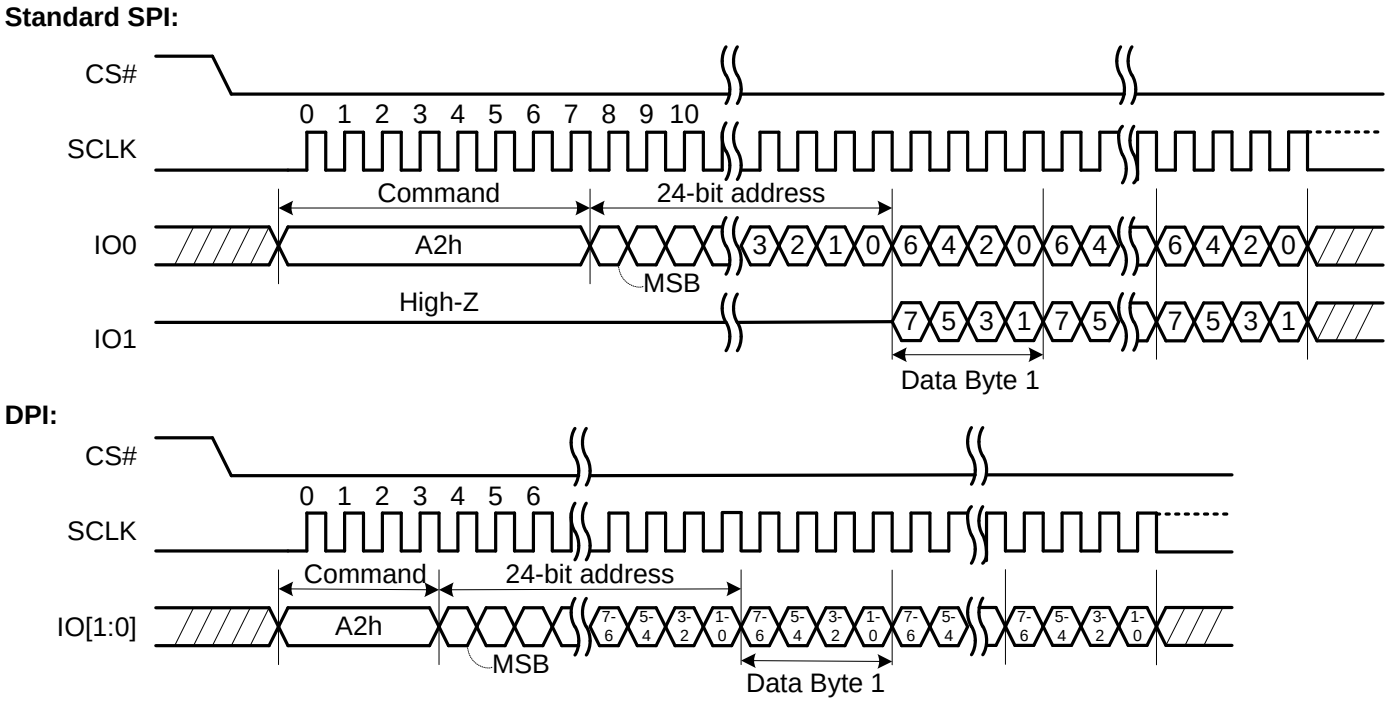


Figure 31: **Dual Input Fast Program (A2h) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).
2. For DPI protocol, C_X=3+$\frac{(A[MAX]+1)}{2}$.

10.9.3. Extended Dual Input Fast Program (D2h)

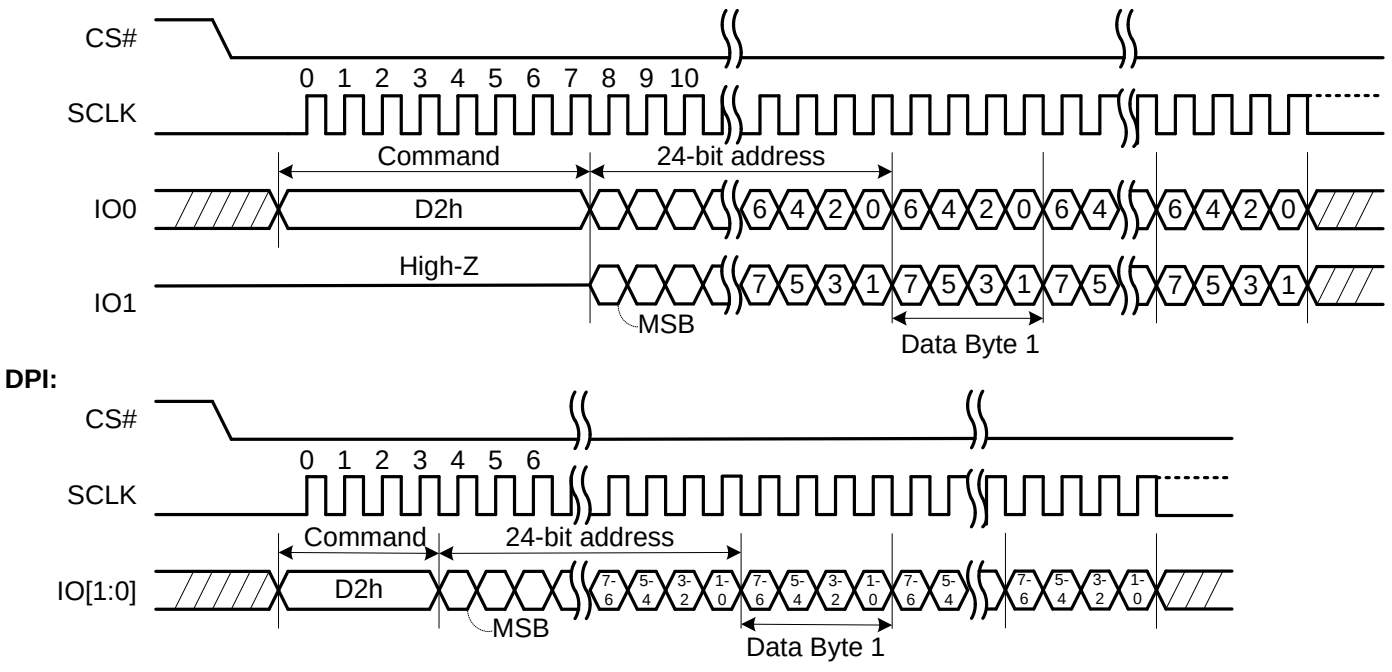


Figure 32: **Extended Dual Input Fast Program (D2h) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{2}$.

2. For DPI protocol, $C_X=3+\frac{(A[MAX]+1)}{2}$.

10.9.4. Quad Input Fast Program (32h/34h)

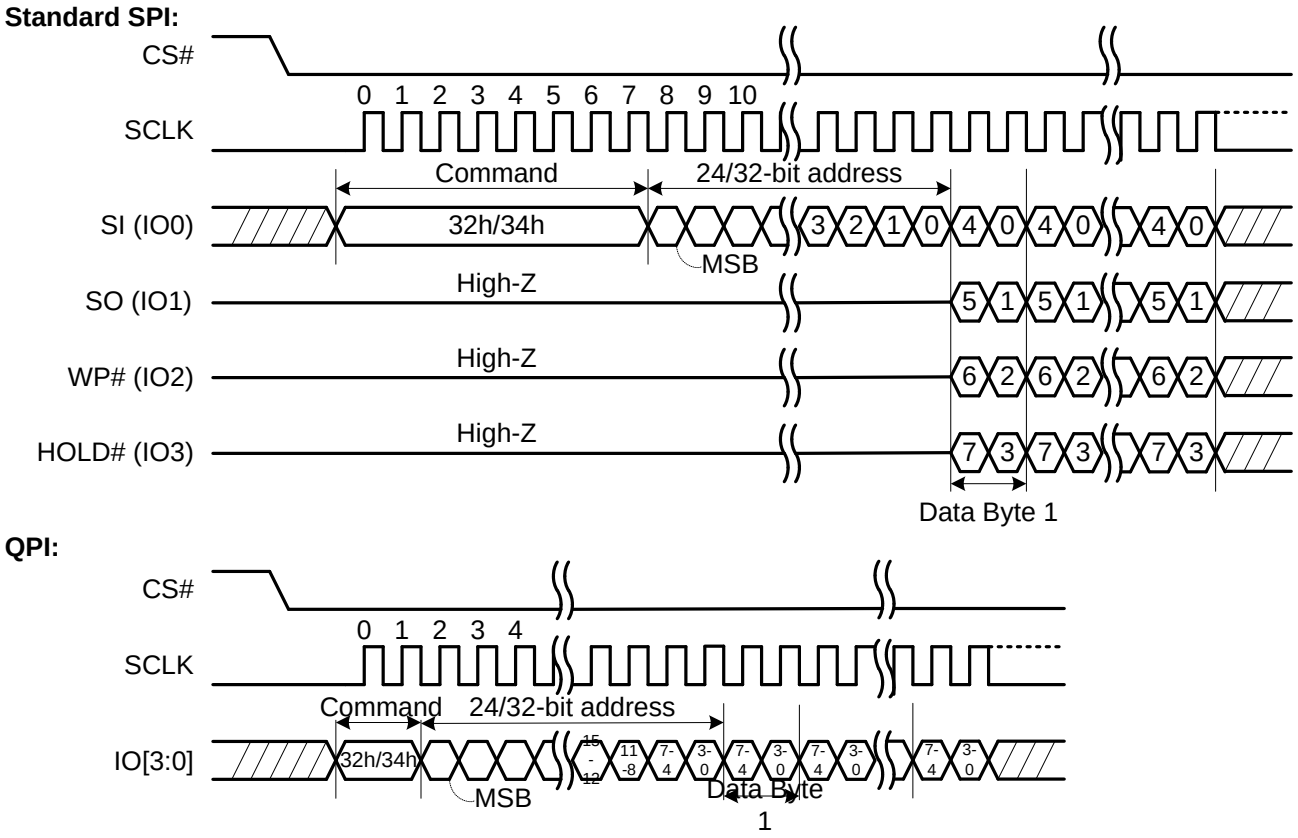


Figure 33: **Quad Input Fast Program (32h/34h) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+(A[MAX]+1)$.

2. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{4}$.

10.9.5. Extended Quad Input Fast Program (38h/3Eh)

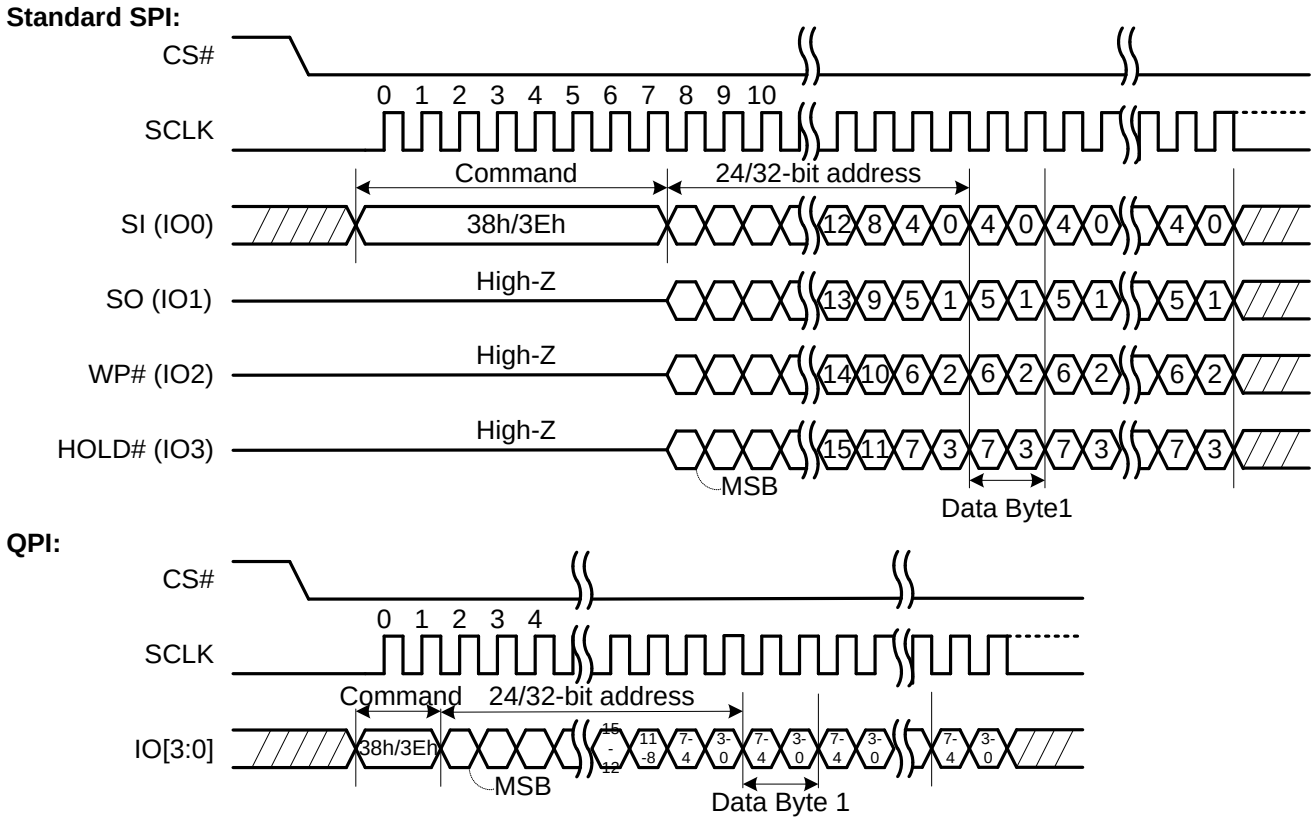


Figure 34: **Extended Quad Input Fast Program (38h/3Eh) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+\frac{(A[MAX]+1)}{4}$.

2. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{4}$.

10.10.Erase Operations

An Erase operation changes 4K/32K/64K bytes of data or the entire main memory array from 0 to 1. Before an Erase operation, the WEL bit must be set to enable the device, otherwise the erase command is ignored and the operation fails with no error bits set.

The command sequence is as follows:

Drive CS# low --> Send command byte --> Send address bytes --> Drive CS# high.

For 20h, 52h and D8h Erase commands, any address within the expected sector or erase is valid for entry, while 60h/C7h commands converts the entire memory array to 1.

After CS# is driven high, a self-timed erase cycle (tSSE, tSE or tBE) is initiated. While the erase cycle is in progress, the WIP bit becomes 1, and WEL bit will be reset to 0 even if the erase operation fails. It is recommended to continuously check the Status Register and Flag Status Register for the status of the operation. After the erase cycle is complete, the WEL bit is reset to 0.

The CS# pin must be driven high exactly at a byte boundary, otherwise the command is ignored. If CS# remains low after the erase command is input, then the erase operation is not executed, WEL remains 1, and error bits are not set.

If a erase command is applied to a protected page, then it is not executed, WEL bit remains 1, and PTE and EE error bits are set.

10.10.1. 4KB Subsector / 32KB Subsector / 64KB Sector Erase (20h/52h/D8h)

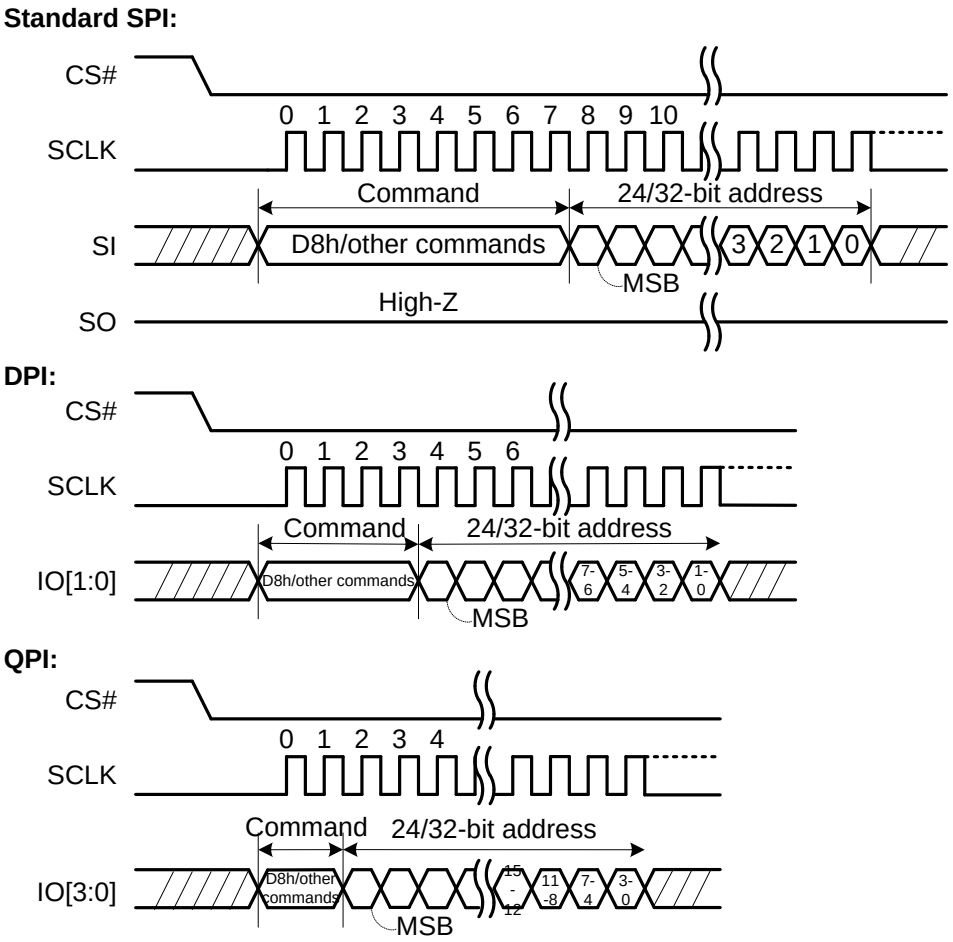


Figure 35: **4KB Subsector / 32KB Subsector / 64KB Sector Erase (20h/52h/D8h) Command Sequence**

Notes:

1. For standard SPI protocol, $C_X=7+(A[MAX]+1)$.
2. For DPI protocol, $C_X=3+\frac{(A[MAX]+1)}{2}$.
3. For QPI protocol, $C_X=1+\frac{(A[MAX]+1)}{4}$.

10.10.2. Bulk Erase (CE) (60h/C7h)

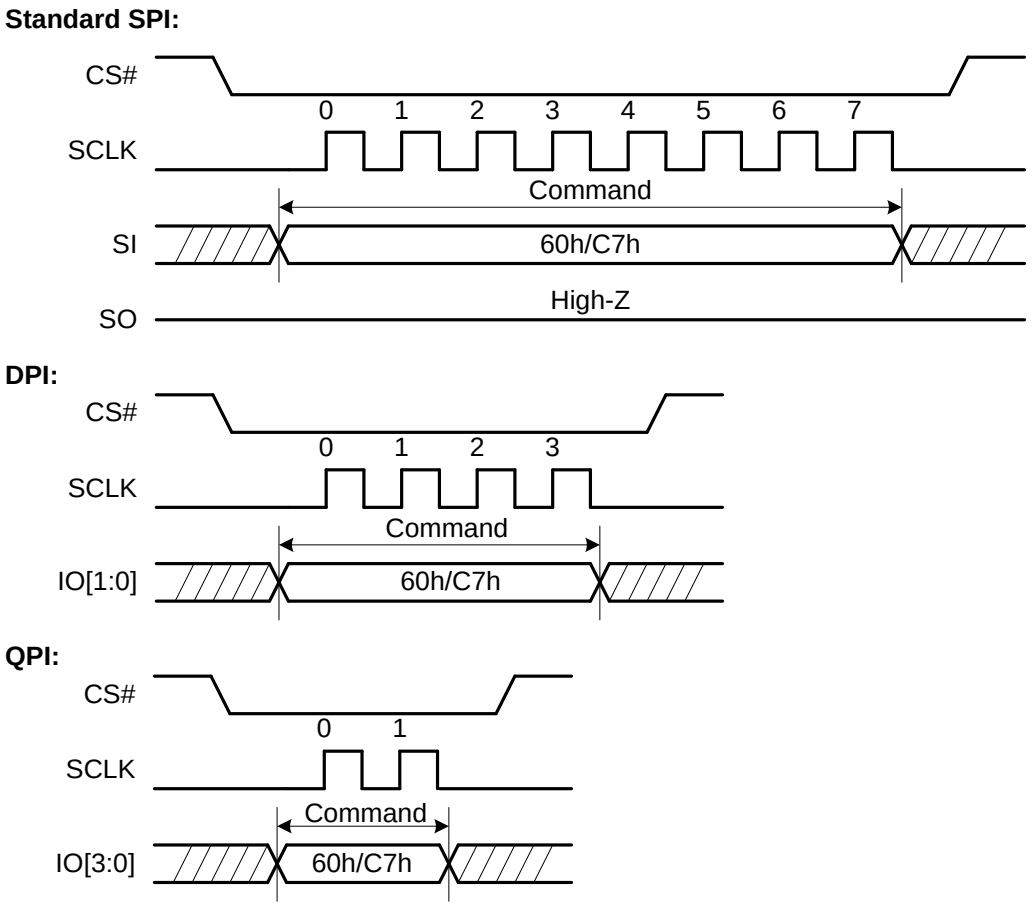


Figure 36: **Bulk Erase (60h/C7h) Command Sequence**

10.11.Suspend/Resume Operations

Program and Erase operations can be interrupted and paused by the Program/Erase Suspend, and resumed by the Program/Erase Resume commands, respectively. A suspended operation can exit the suspend state and continue to execute if Program/Erase Resume command is issued. When resuming from a suspended Erase state, the Volatile Lock Bit Register is not checked.

The command sequence is as follows:

Drive CS# low --> Send command byte --> Drive CS# high.

Program Suspsend asserts SUS2 bit to 1, while Erase Suspend asserts SUS1 bit to 1. SUS1or SUS2 will be clear if program or erase operation has done before the suspend latency arrived or device gets suspend resumed command. The SUS1 and SUS2 bits are volatile and are reset if the device is powered up.

While the device is in Program suspension, any Read command can be accepted; the page in program suspend state should be excluded from the read address range, otherwise indeterminate data is output.

While the device is in Erase suspension, any Program or Read command can be accepted for a non-suspension address range. Reading from an address range in erase suspension may output indeterminate data; program operations on an address range in erase suspension is ignored with PE bit set. Besides, in Erase suspension, all commands can be accepted except:

4KB Sector / 32KB Block / 64KB Block Erase,

Write Status Register,

Write Nonvolatile Configuration Register,

Program OTP.

When Program/Erase Suspend commands can be nested once.

10.11.1. Program/Erase Suspend and Resume (75h/7Ah)

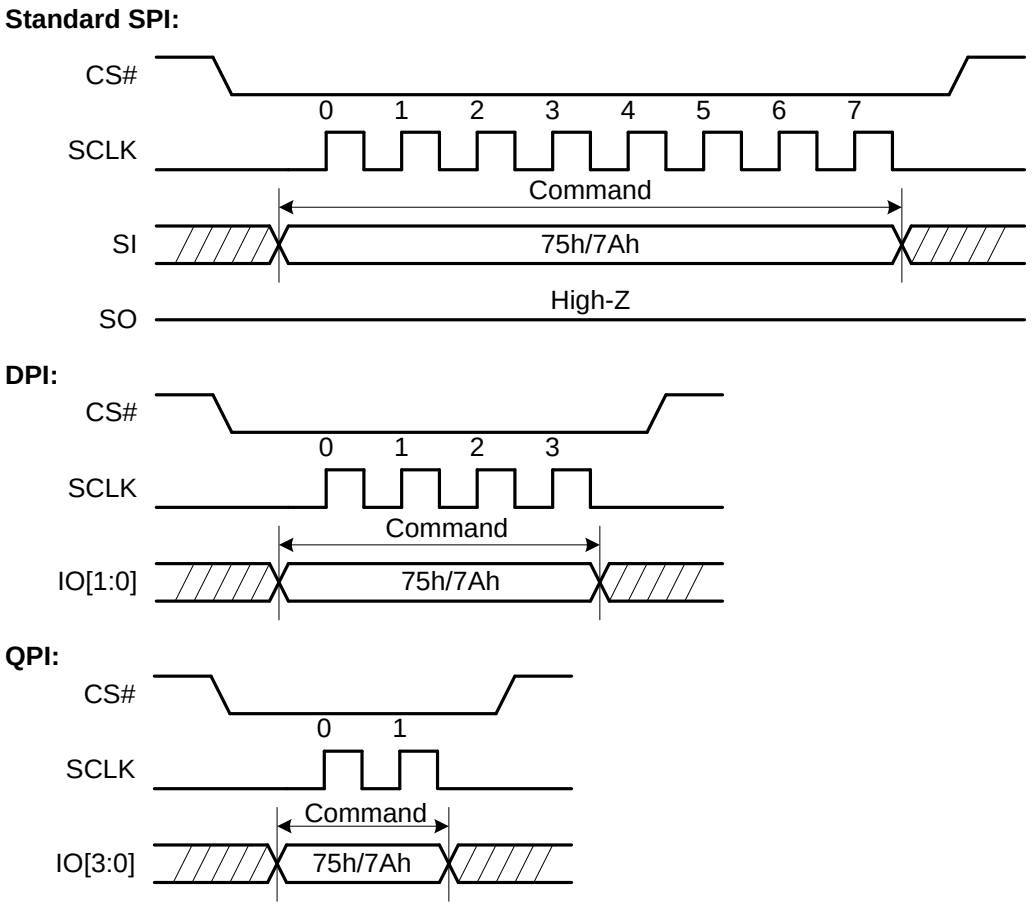


Figure 37: **Program/Erase Suspend and Resume (75h/7Ah) Command Sequence**

10.12.One-Time Programmable (OTP) Operations

10.12.1. Read OTP Area Security Registers (4Bh)

To perform read operation, the command sequence is as folows:

Drive CS# low --> Shift in command byte --> Shift in address bytes --> Shift out OTP data starting from the specified address --> The host may terminate the command by driving CS# high at any time during data output.

The maximum clock frequency of OTP read is fC. The address can point to any byte location in the OTP area. After each byte is shifted out, the address automatically increments to the next byte location. After the entire OTP area is shifted out, the output data does not roll back; rather, after the last byte is reached, the device continues to output data at the address of the last byte.

The address definition of 4Bh command is specified in Section *8.4 OTP Area* Security Register.

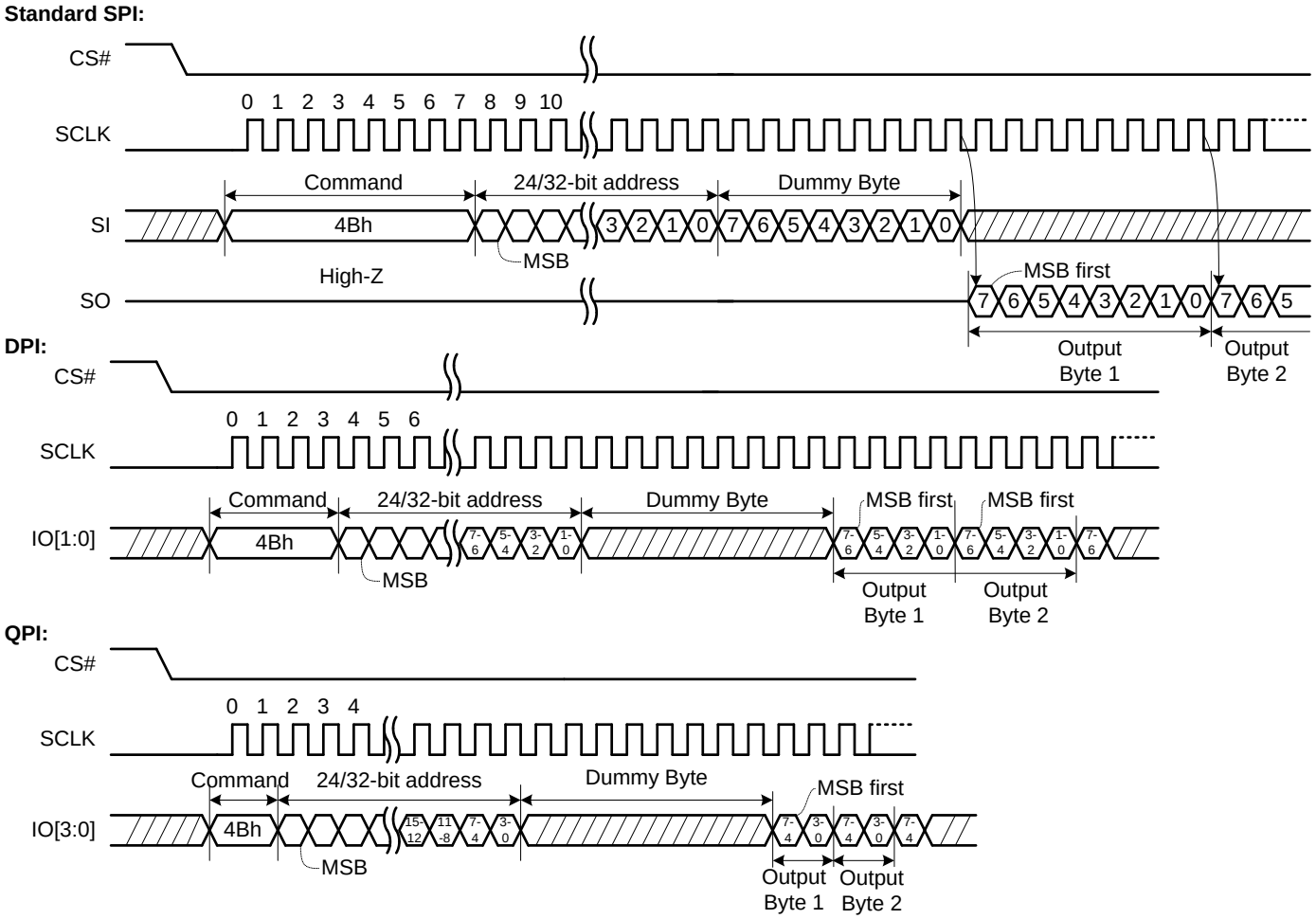


Figure 38: **Read Security Registers (4Bh) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).
2. For DPI protocol, C_X=3+$\frac{(A[MAX]+1)}{2}$.
3. For QPI protocol, C_X=1+$\frac{(A[MAX]+1)}{4}$.

10.12.2. Program OTP Area Security Registers (42h)

The Program Security Register command programs data to a specified location in the OTP area Security Register. The WEL bit must be set to enable the device for programming operation, otherwise the program command is ignored with Flag Status Register bits unchanged. Attempting to program a memory location that has previously been programmed but not erased may corrupt the data.

The command sequence is as follows:

Drive CS# low --> Send in command byte --> Send in address bytes --> Send in data -> Drive CS# high.

The address definition of 42h command is specified in *8.4 OTP Area* Security Register; the program data does not roll back so that after the last byte of the current OTP area is reached, all subsequent data bytes are discarded.

After CS# is driven high, a self-timed Program Security Registers cycle (tPP) is initiated. While the program cycle is in progress, the WIP bit becomes 1, and WEL bit will be reset to 0 even if the program operation fails. It is recommended to continuously check the Status Register and Flag Status Register for the status of the operation. After the programming cycle is complete, the WEL bit is reset to 0.

The CS# pin must be driven high exactly at a byte boundary, otherwise the command is ignored. If CS# remains low after all program data is input, then the program operation is not executed, WEL remains 1, and error bits

are not set. If the program operation is timeout, the WEL bit is reset to 0 and PE bit is set to 1.

If an OTP Program command is applied to a register which is permanently locked, then it is not executed, WEL bit remains 1, and PTE and PE error bits are set.

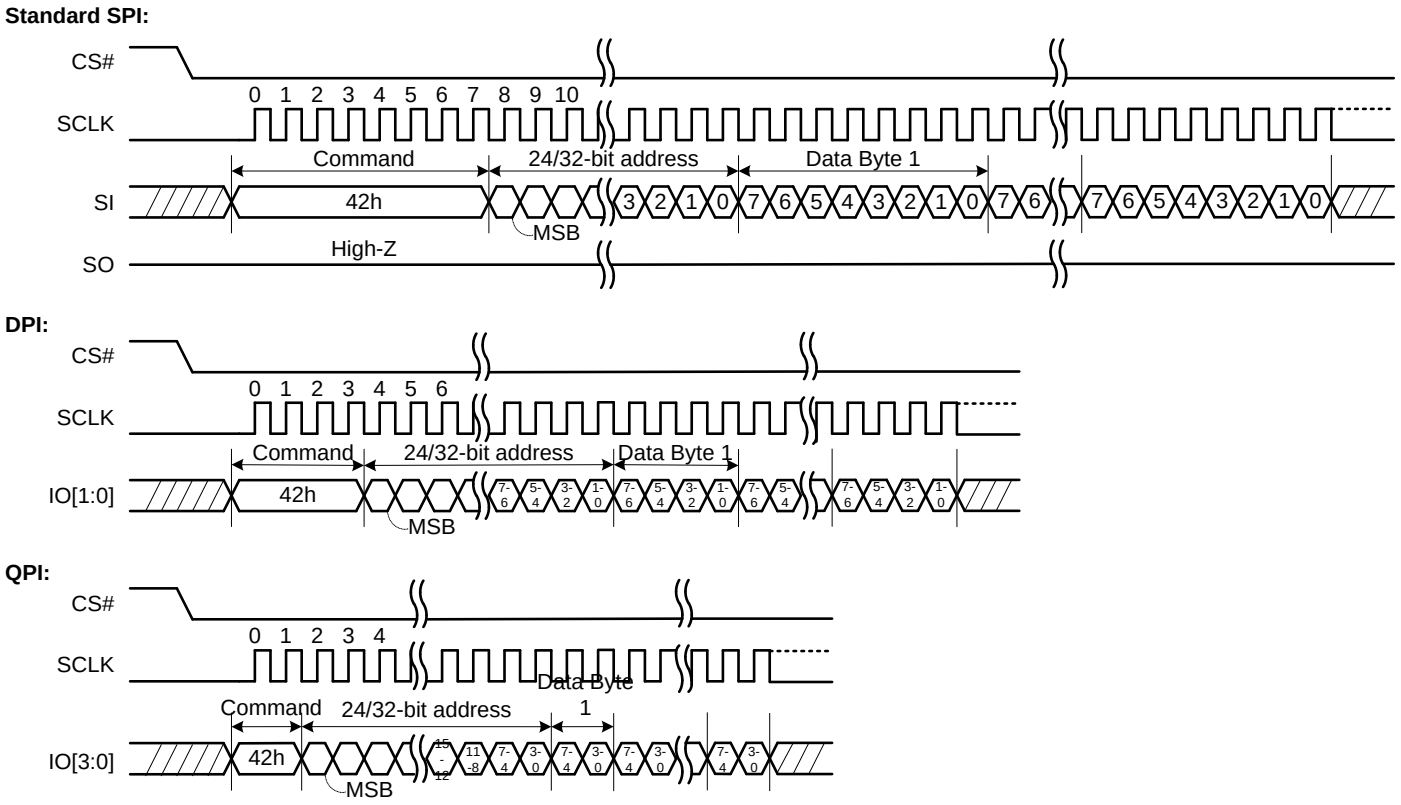


Figure 39: **Program OTP Area Security Register (42h) Command Sequence**

Notes:

1. For standard SPI protocol, C_X=7+(A[MAX]+1).
2. For DPI protocol, C_X=3+$\frac{(A[MAX]+1)}{2}$.
3. For QPI protocol, C_X=1+$\frac{(A[MAX]+1)}{4}$.

10.13.4-Byte Address Mode Operations

10.13.1. Enter 4-Byte Address Mode (EN4B B7h)

The B7h command enables address bits 31 through 24, allowing the user to access memory space beyond 128Mbits. The default state of the device is 3-Byte Address mode. The B7h command sets ADS bit to 1, indicating the device is in 4-Byte Address mode, and the address domain of a command should occupy 32 bits rather than 24 bits.

The command sequence is as follows:

Drive CS# low --> Send in command byte --> Drive CS# high.

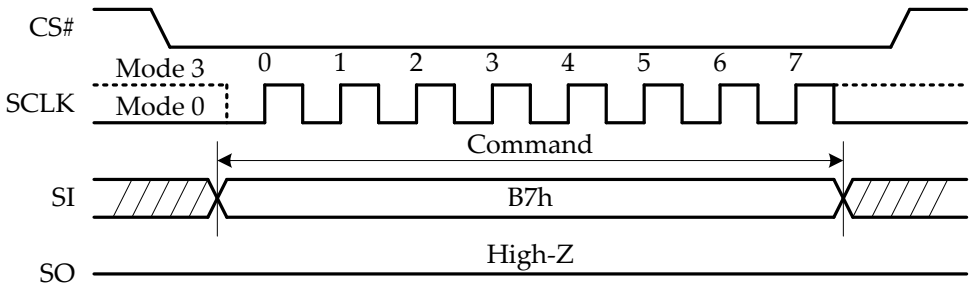


Figure 40: **Enter 4-Byte Address Mode (B7h) Command Sequence**

10.13.2. Exit 4-Byte Address Mode (EX4B E9h)

The E9h command brings the device from 4-Byte Address mode back to 3-Byte Address mode, and clears ADS bit to 0 to indicate the current address mode.

The command sequence is as follows:

Drive CS# low --> Send in E9h command byte --> Drive CS# high.

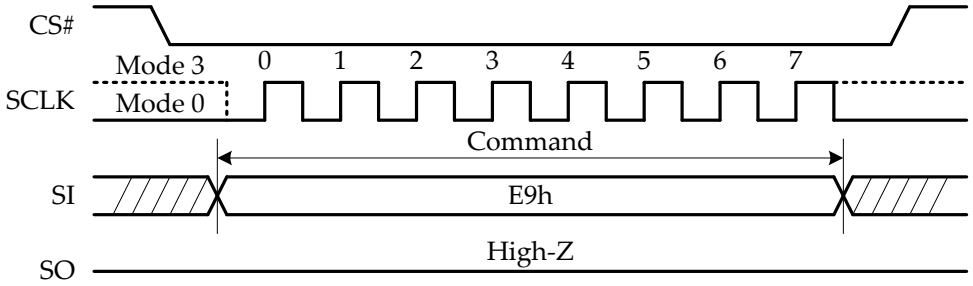


Figure 41: **Exit 4-Byte Address Mode (E9h) Command Sequence**

10.14.QPI Protocol Operations

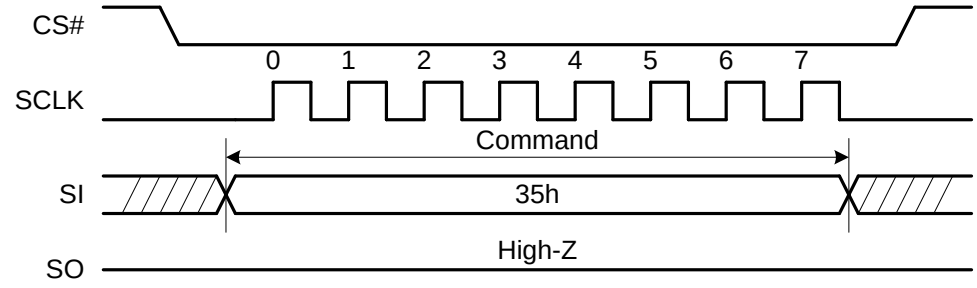
The 35h and F5h commands brings the device into and out of QPI mode, respectively. In order for these commands to be accepted, the WEL bit must be 0.

The command sequence is as follows:

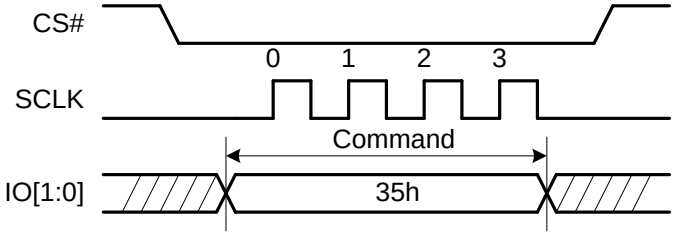
Drive CS# low --> Send in command byte --> Drive CS# high.

10.14.1. Enter Quad Input/Output Mode (35h)

Standard SPI:



DPI:



QPI:

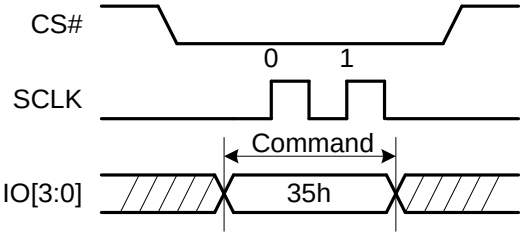


Figure 42: **Enter Quad Input/Output Mode (35h) Command Sequence**

10.14.2. Reset Quad Input/Output Mode (F5h)

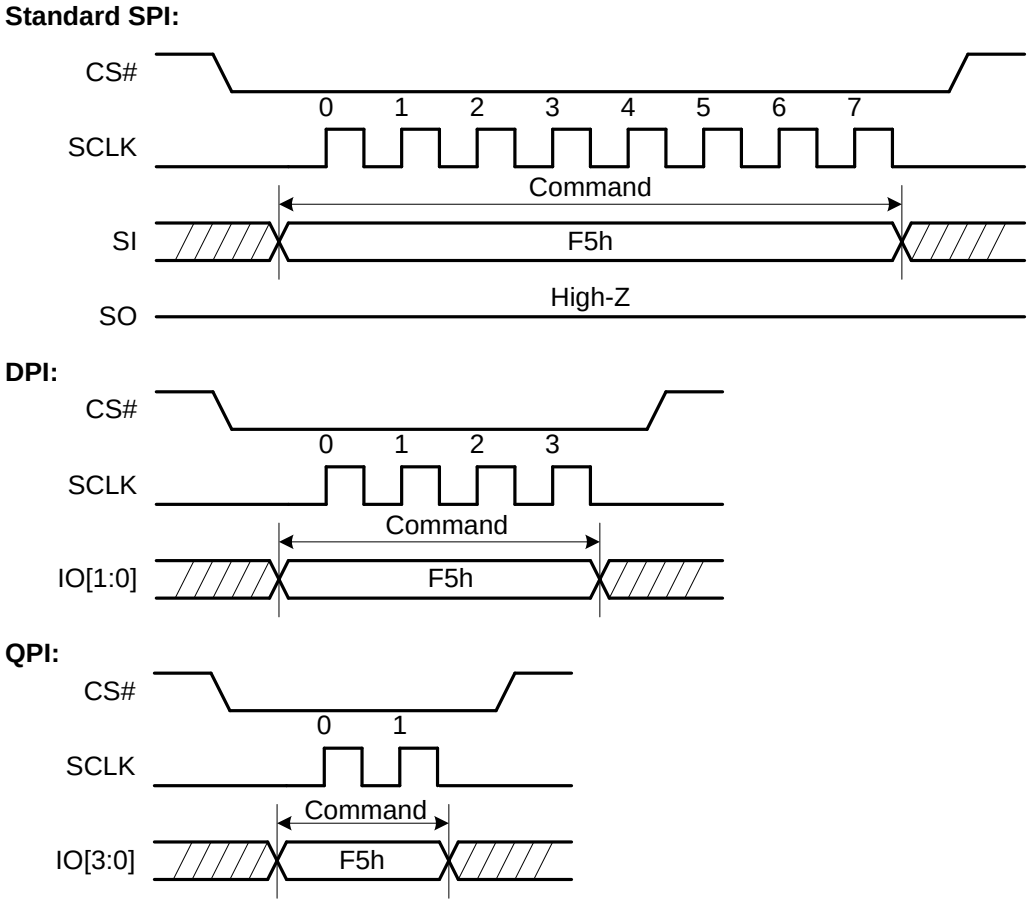


Figure 43: **Reset Quad Input/Output Mode (F5h) Command Sequence**

10.15.Deep Power-Down Operations

10.15.1. Deep Power-Down (DP) (B9h)

DP command is the only way to bring the device into Deep Power-Down mode. In this mode, the supply current is reduced from standby current I_{CC1} to I_{CC2}. This command offers an extra software protection mechanism that protects the device from all Write, Program or Erase commands.

The command sequence is as follows:

Drive CS# low --> Send in command byte --> Drive CS# high --> After a delay of tDP --> Supply current is reduced to I_{CC2}.

The CS# pin must be driven high after the eighth bit of the command input, otherwise the operation is not executed. As soon as CS# is driven high, the device first returns to standby mode if no internal Write, Program or Erase operation is in progress. After a delay of t_{DP}, the device enters Deep Power-Down Mode and power consumption is greatly reduced.

In deep power-down mode, the WEL bit remains unchanged, and no error bits are set. In this state, the device ignores all commands except:

"Release from Deep Power-Down" command,

Hardware reset,

Power-loss rescue sequence commands.

Release from Deep Power-Down command and power-down can release the device from Deep Power-Down mode and bring it back to standby mode. While an Write, Program or Erase operation is in progress, the B9h command is ignored by the device.

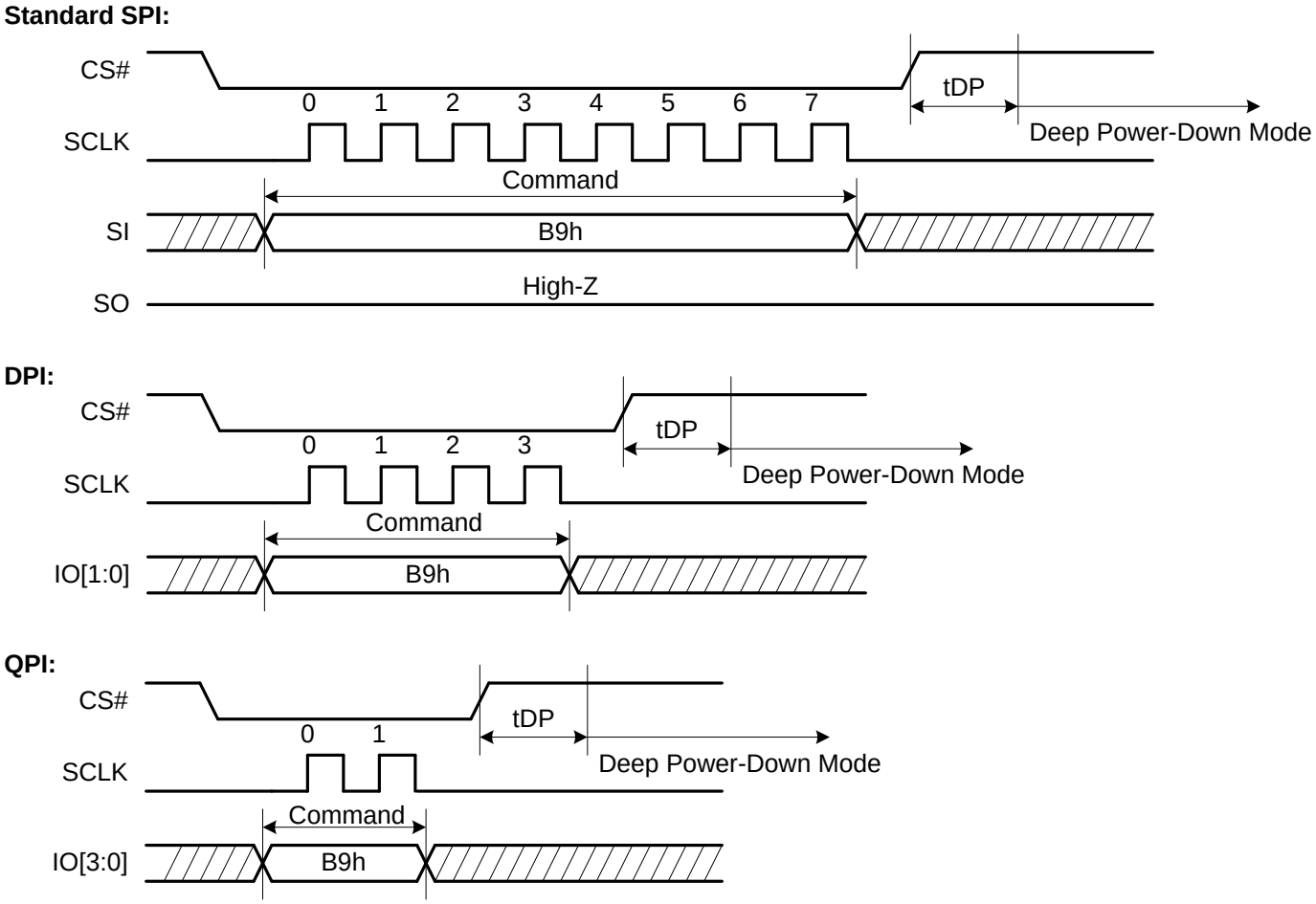


Figure 44: **Deep Power-Down (DP) (B9h) Command Sequence**

10.15.2. Release from Deep Power-Down (ABh)

The ABh command releases the device from Deep Power-Down state.

The command sequence is follows:

Drive CS# low --> Send in command byte --> Drive CS# high --> After a delay of tRDP --> The device enters standby mode.

If the device is previously in Deep Power-Down mode, then after CS# transitions high, it takes tRDP before the device resumes normal operation and other commands are accepted. The CS# pin must remain high during tRDP; if the device is not previously in Deep Power-Down mode, then the transition to normal operation is immediate after CS# is deasserted.

If the ABh command is issued while a Write, Program or Erase operation is in progress, the command is ignored.

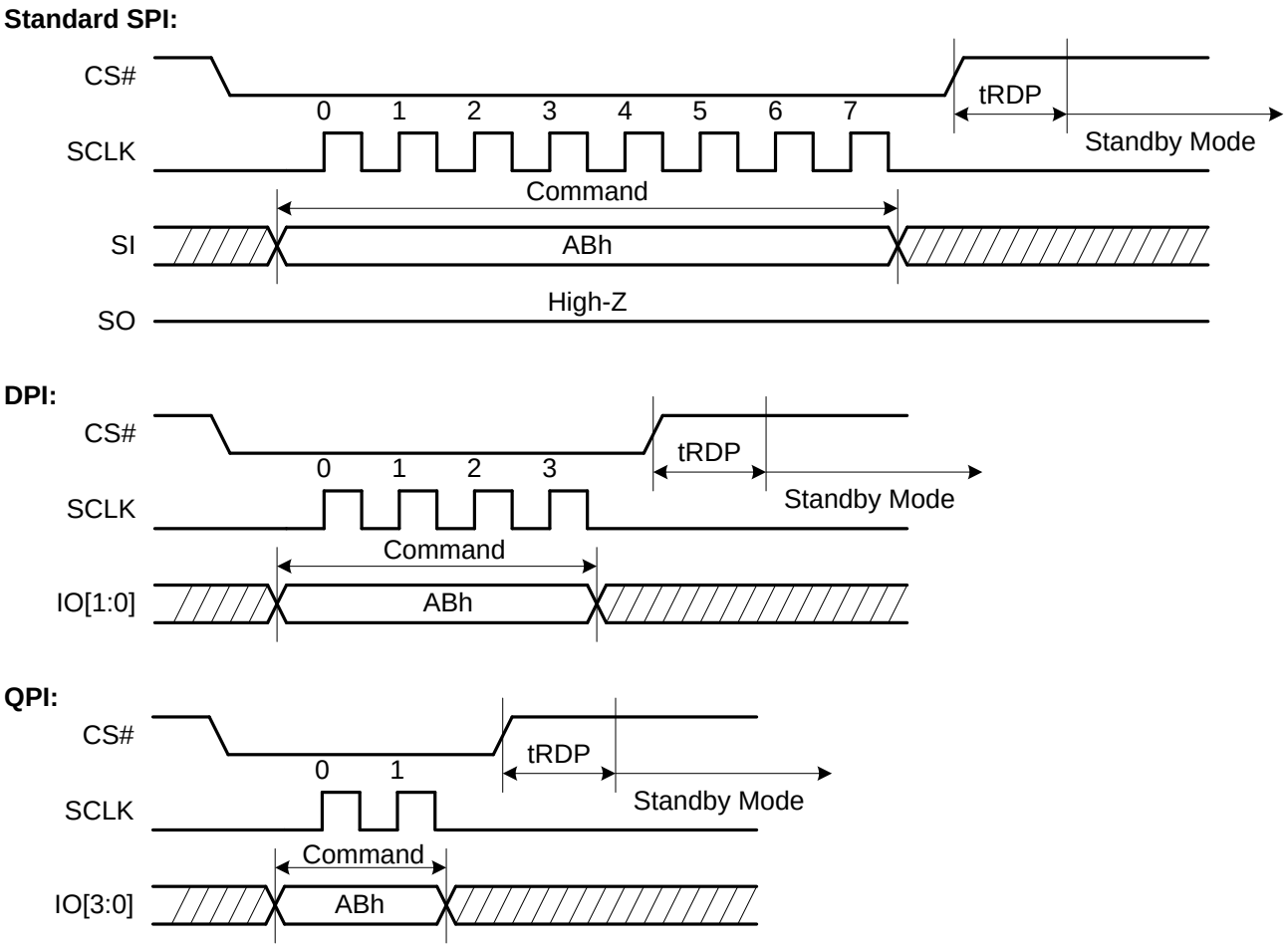


Figure 45: **Release from Deep Power-Down (ABh) Command Sequence**

10.16.Advanced Sector Protection Operations

Advanced sector protection mechanism is implemented via a series of commands, as is defined below.

10.16.1. Read Sector Protection (2Dh)

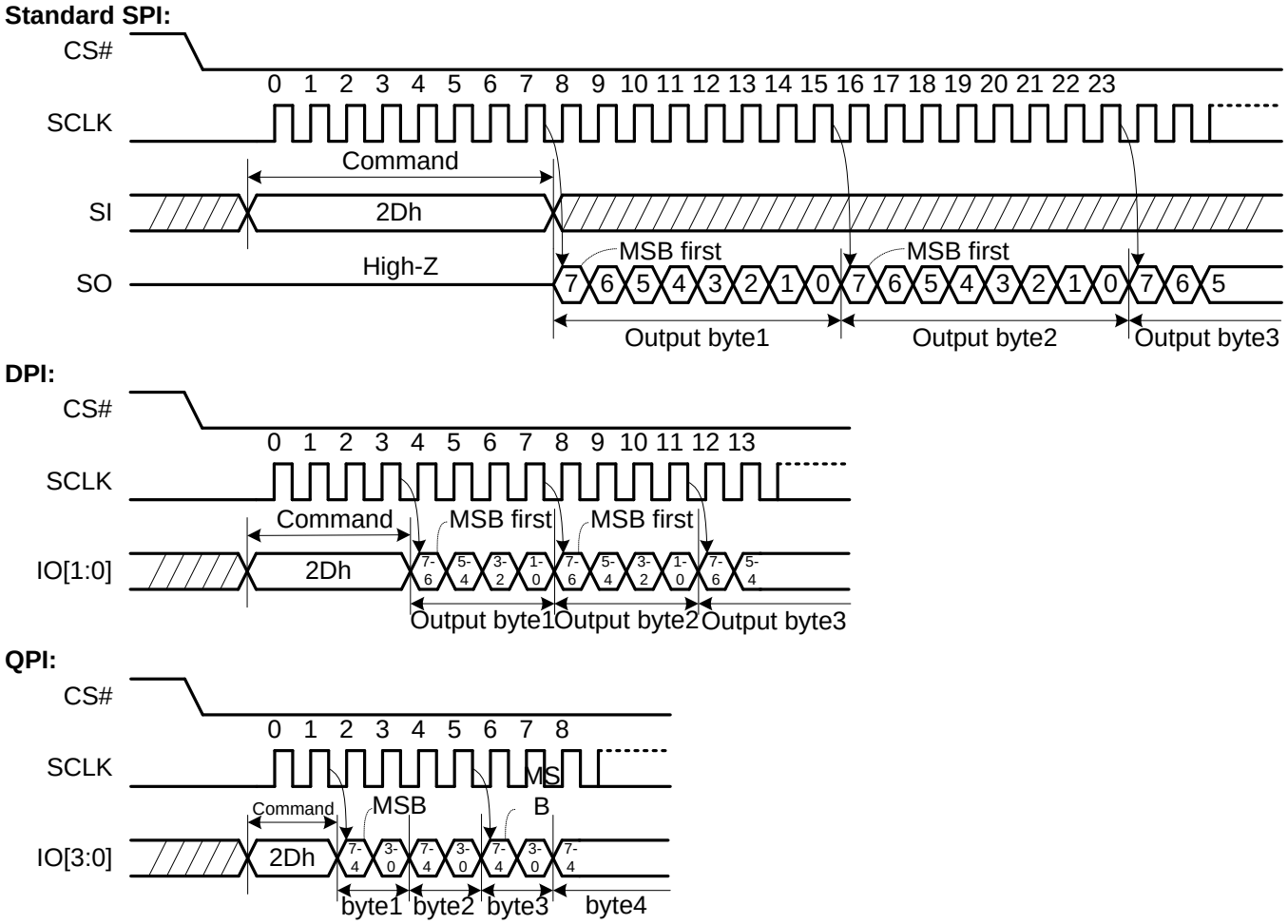


Figure 46: **Read Sector Protection (2Dh) Command Sequence**

10.16.2. Program Sector Protection (2Ch)

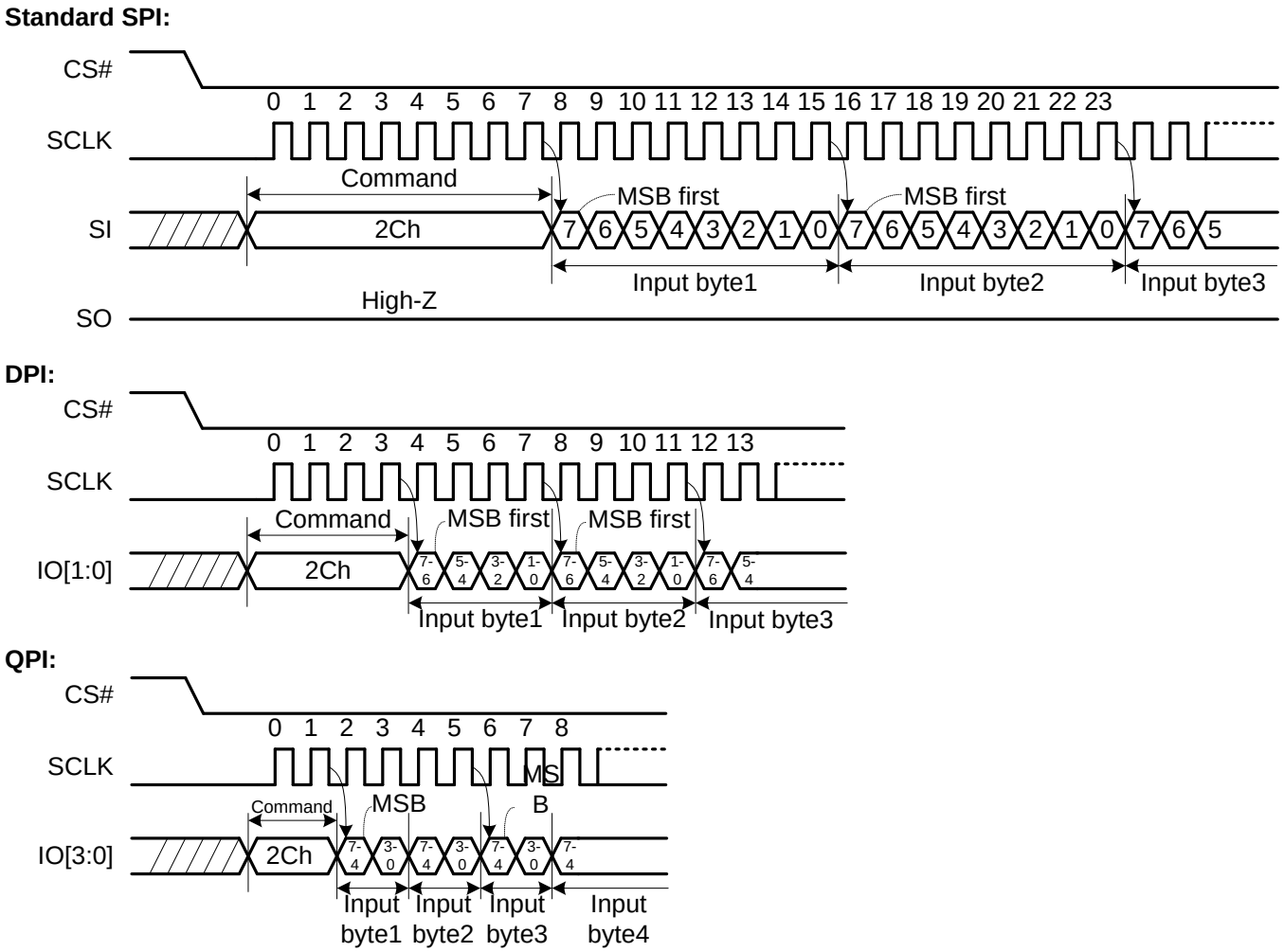


Figure 47: **Program Sector Protection (2Ch) Command Sequence**

10.16.3. Read Volatile Lock Bits (E8h)

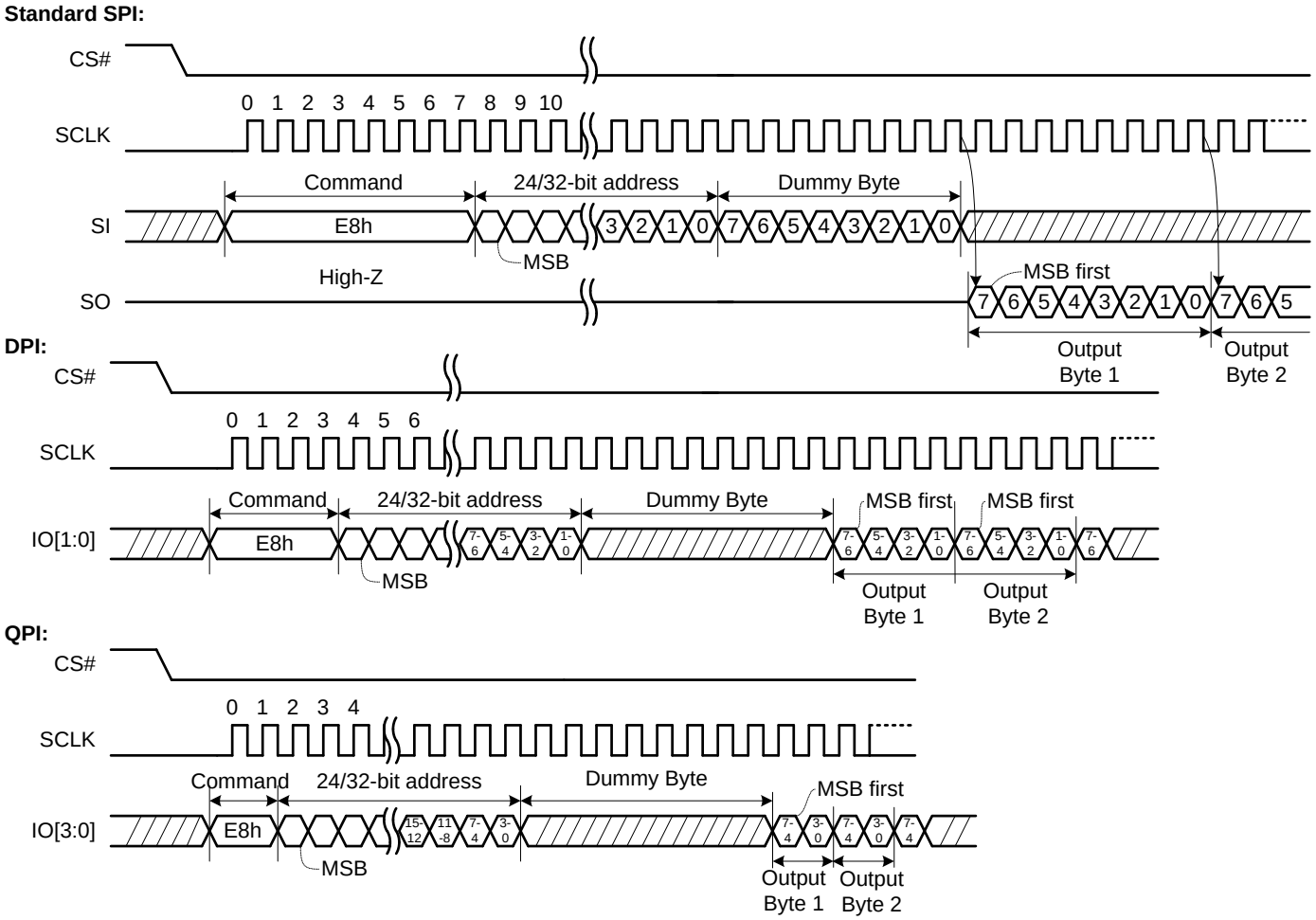
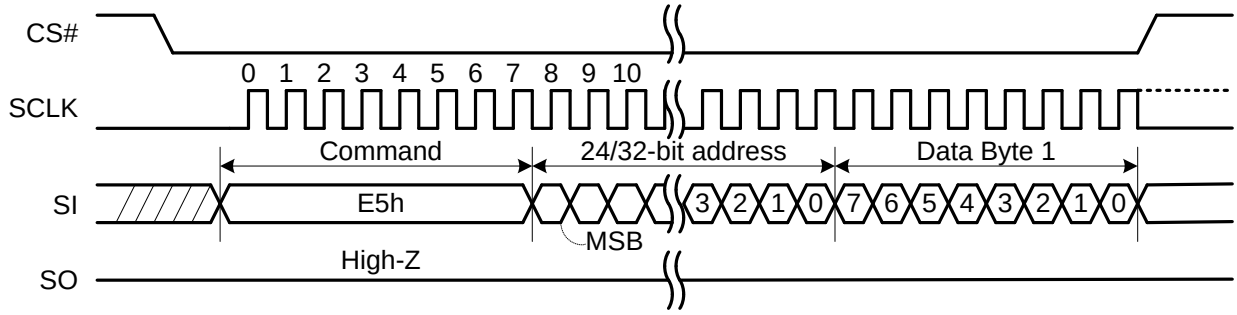


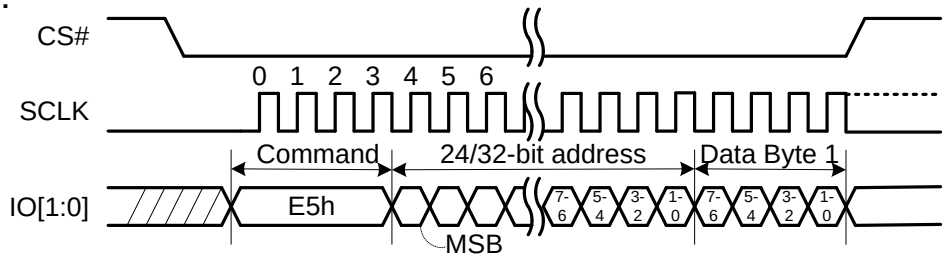
Figure 48: **Read Volatile Lock Bits (E8h) Command Sequence**

10.16.4. Write Volatile Lock Bits (E5h)

Standard SPI:



DPI:



QPI:

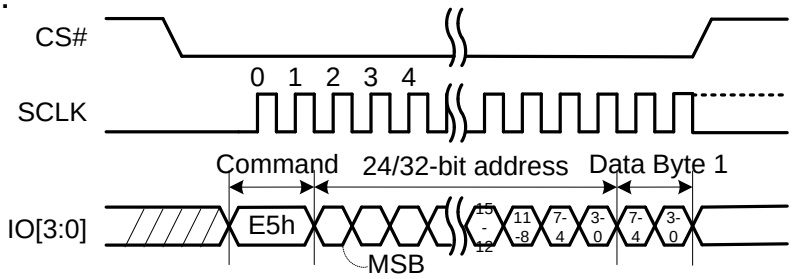


Figure 49: **Write Volatile Lock Bits (E5h) Command Sequence**

10.16.5. Read Nonvolatile Lock Bits (E2h)

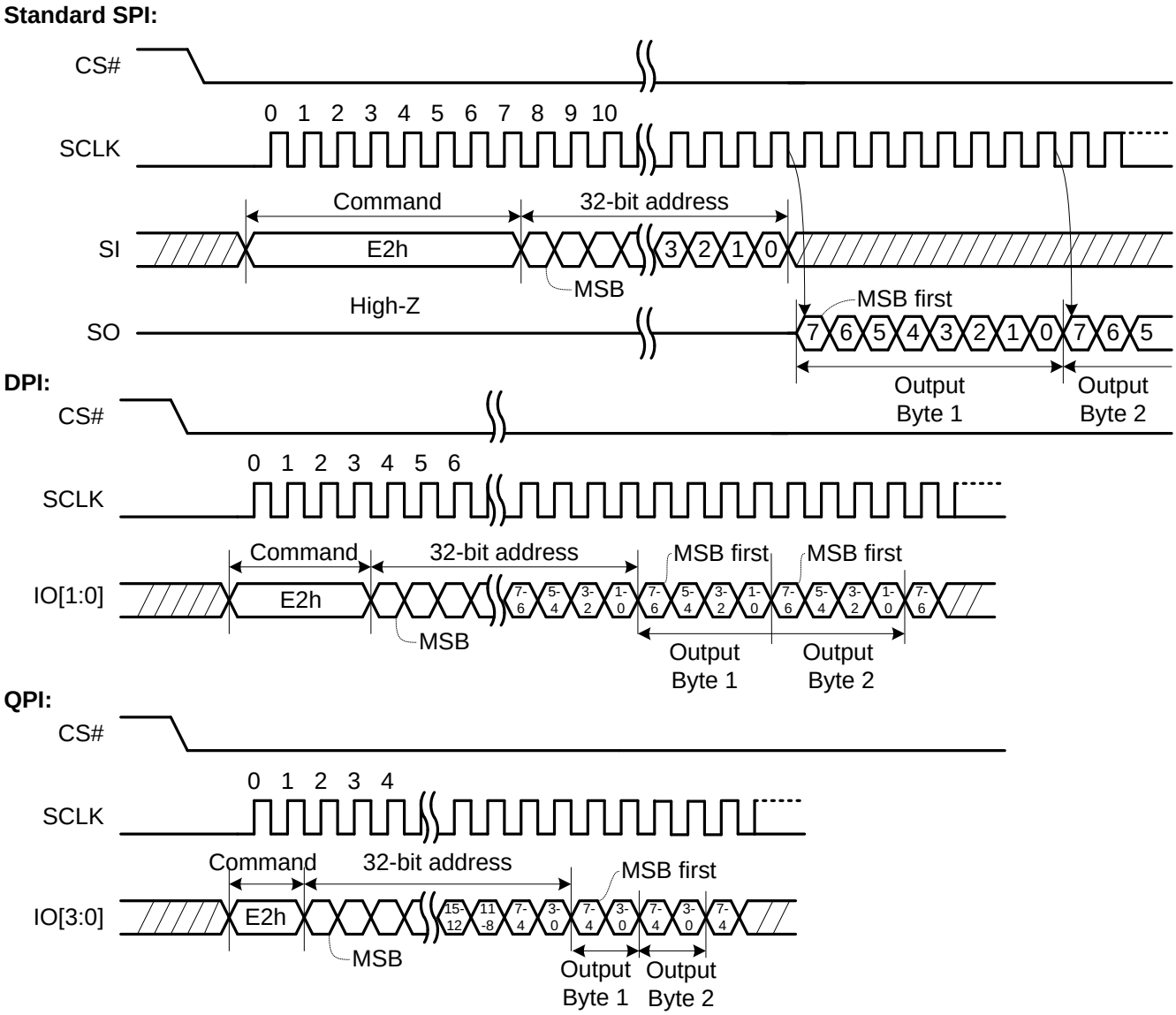
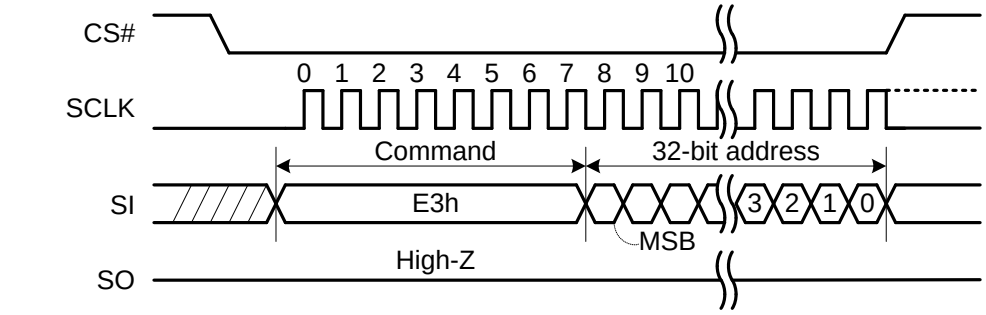


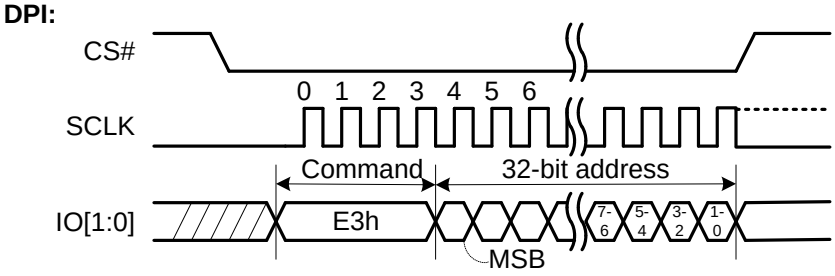
Figure 50: **Read Nonvolatile Lock Bits (E2h) Command Sequence**

10.16.6. Write Nonvolatile Lock Bits (E3h)

Standard SPI:



DPI:



QPI:

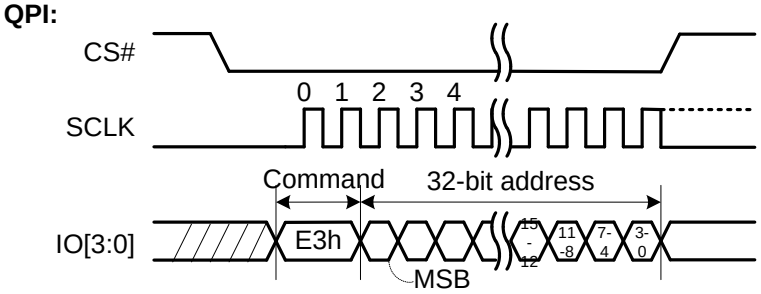


Figure 51: **Write Nonvolatile Lock Bits (E3h) Command Sequence**

10.16.7. Erase Nonvolatile Lock Bits (E4h)

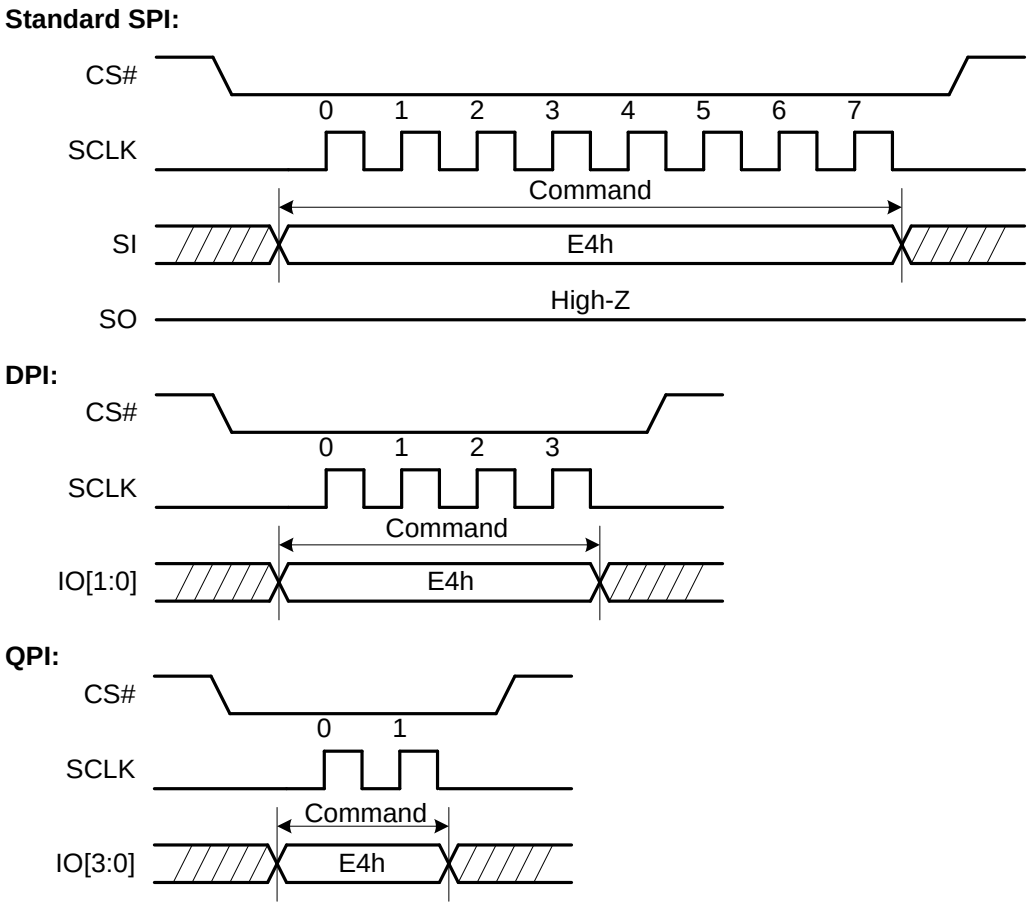


Figure 52: **Erase Nonvolatile Lock Bits (E4h) Command Sequence**

10.16.8. Read Global Freeze Bit (A7h)

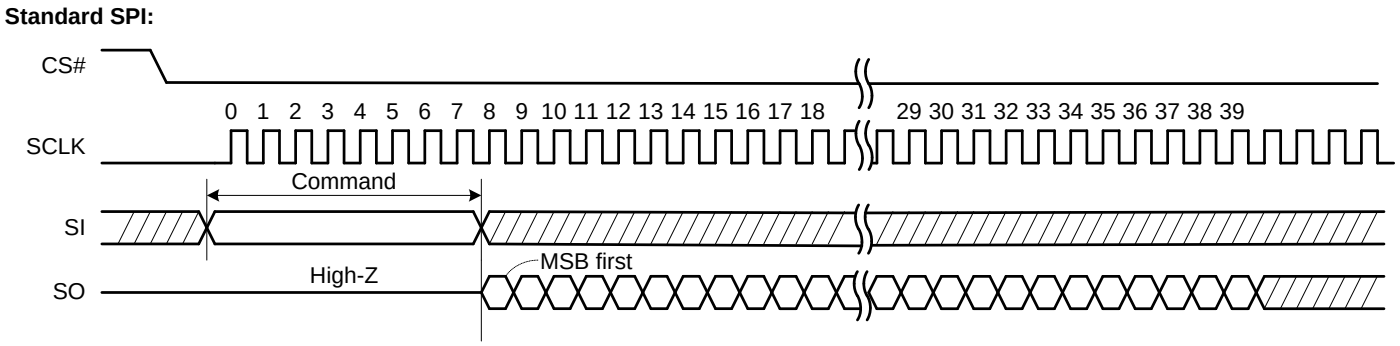


Figure 53: **Read Global Freeze Bit (A7h) Command Sequence**

10.16.9. Write Global Freeze Bit (A6h)

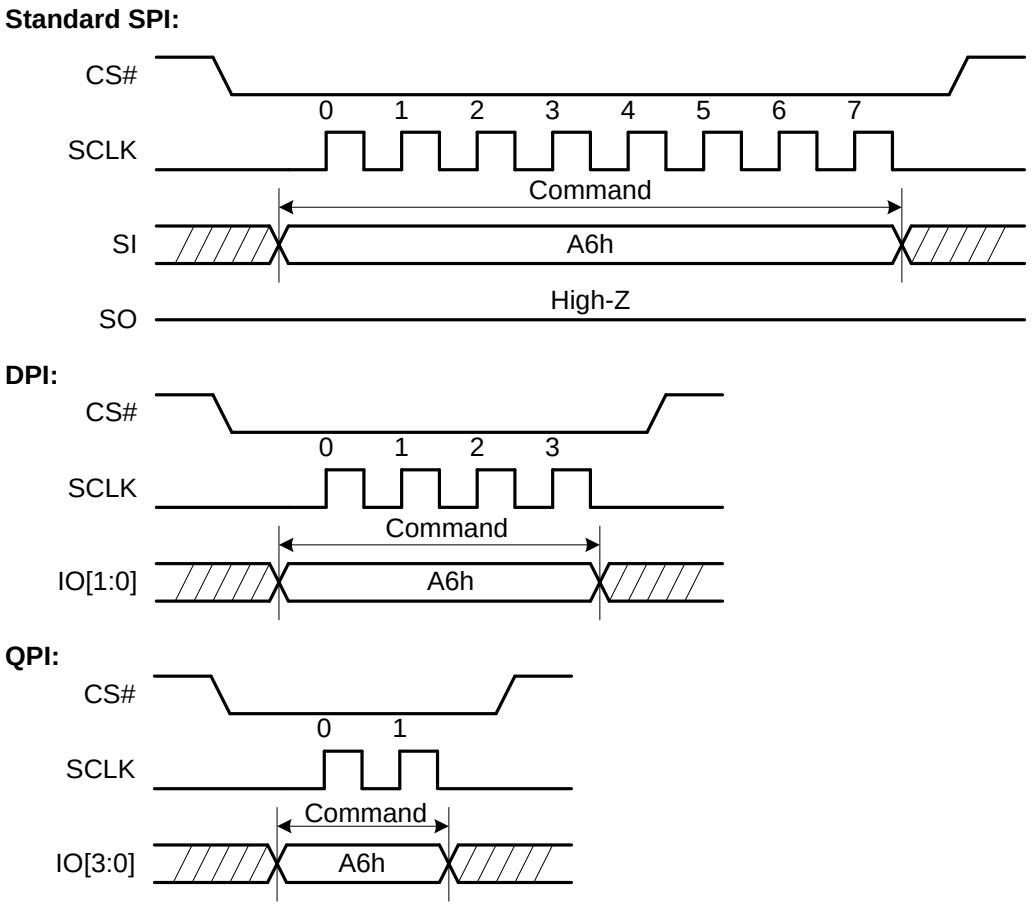


Figure 54: **Write Global Freeze Bit (A6h) Command Sequence**

10.16.10. Read Password (27h)

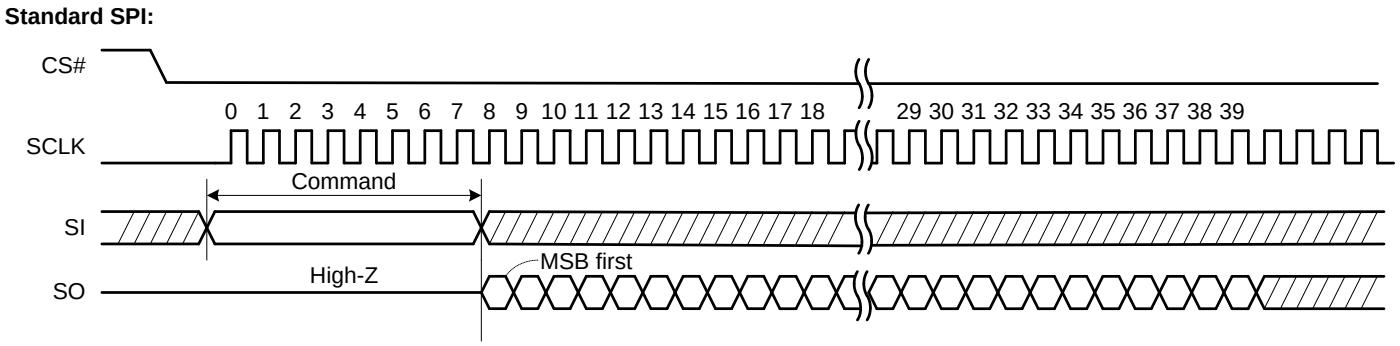
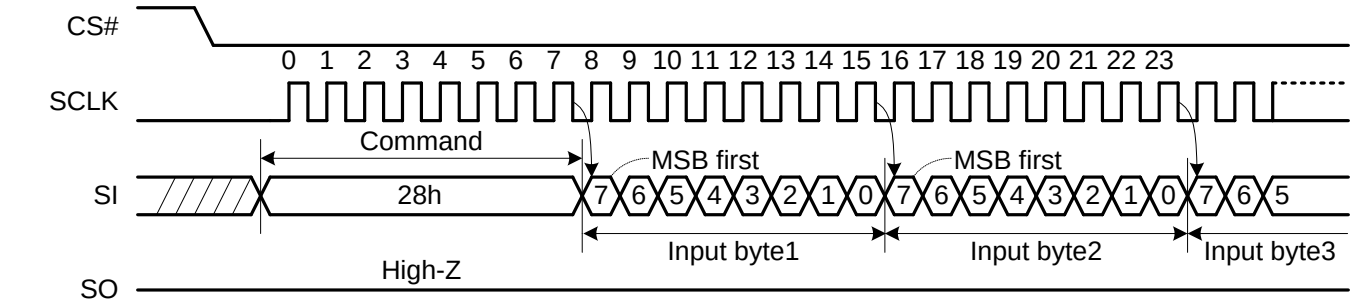


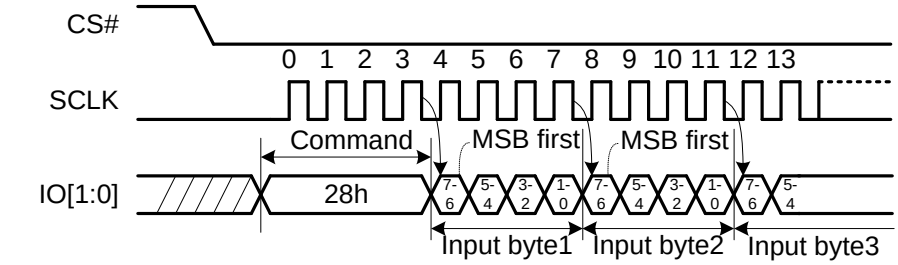
Figure 55: **Read Password (27h) Command Sequence**

10.16.11. Write Password (28h)

Standard SPI:



DPI:



QPI:

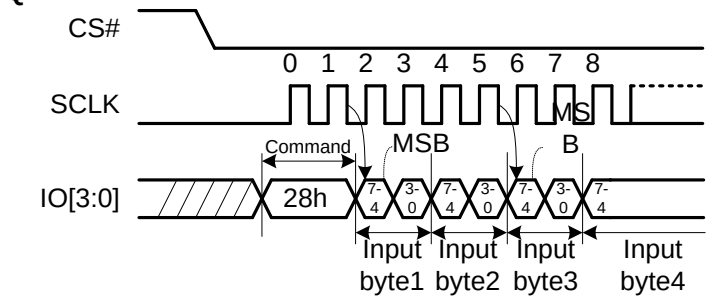
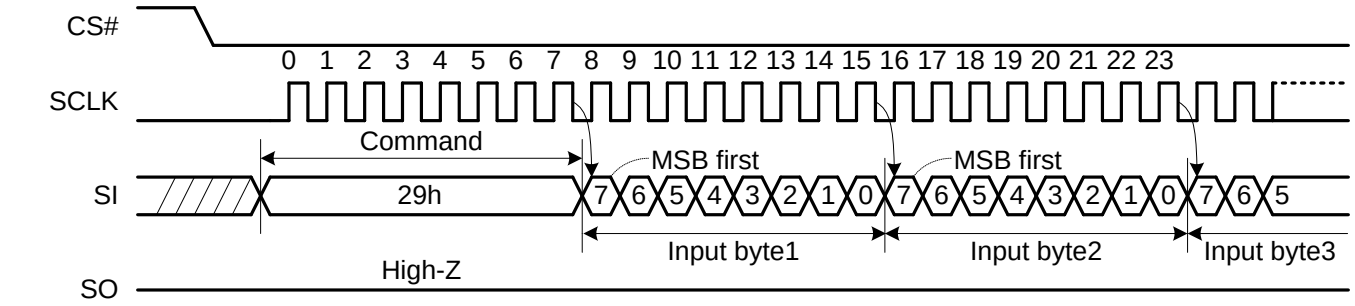


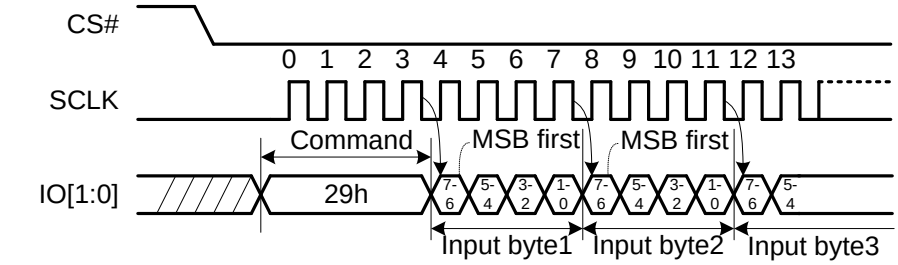
Figure 56: **Write Password (28h) Command Sequence**

10.16.12. Unlock Password (29h)

Standard SPI:



DPI:



QPI:

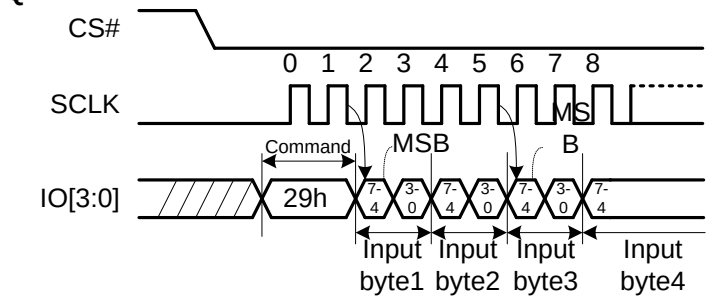


Figure 57: **Unlock Password (29h) Command Sequence**

10.16.13. 4-Byte Read Volatile Lock Bits (E0h)

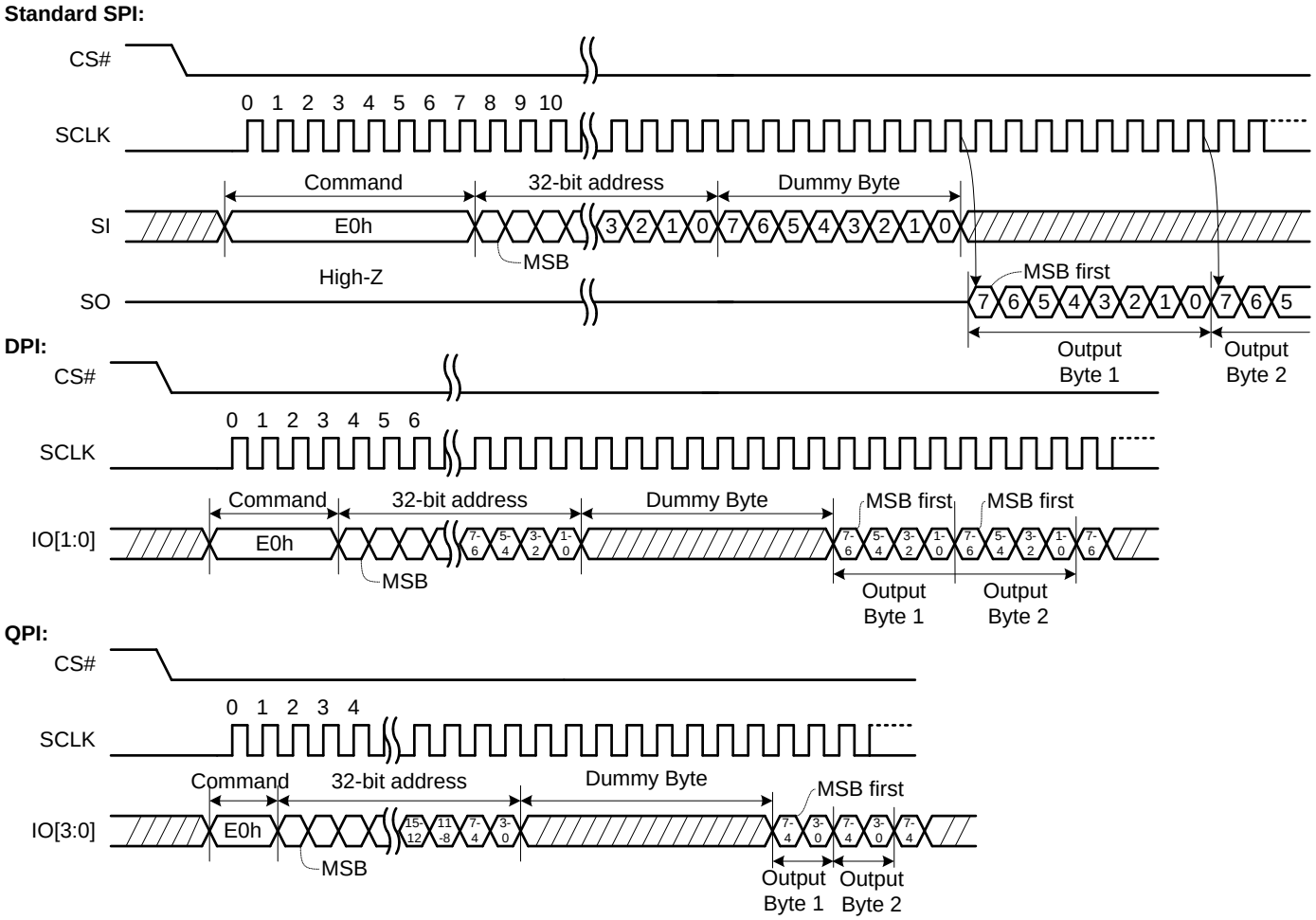


Figure 58: **4-Byte Read Volatile Lock Bits (E0h) Command Sequence**

10.16.14. 4-Byte Write Volatile Lock Bits (E1h)

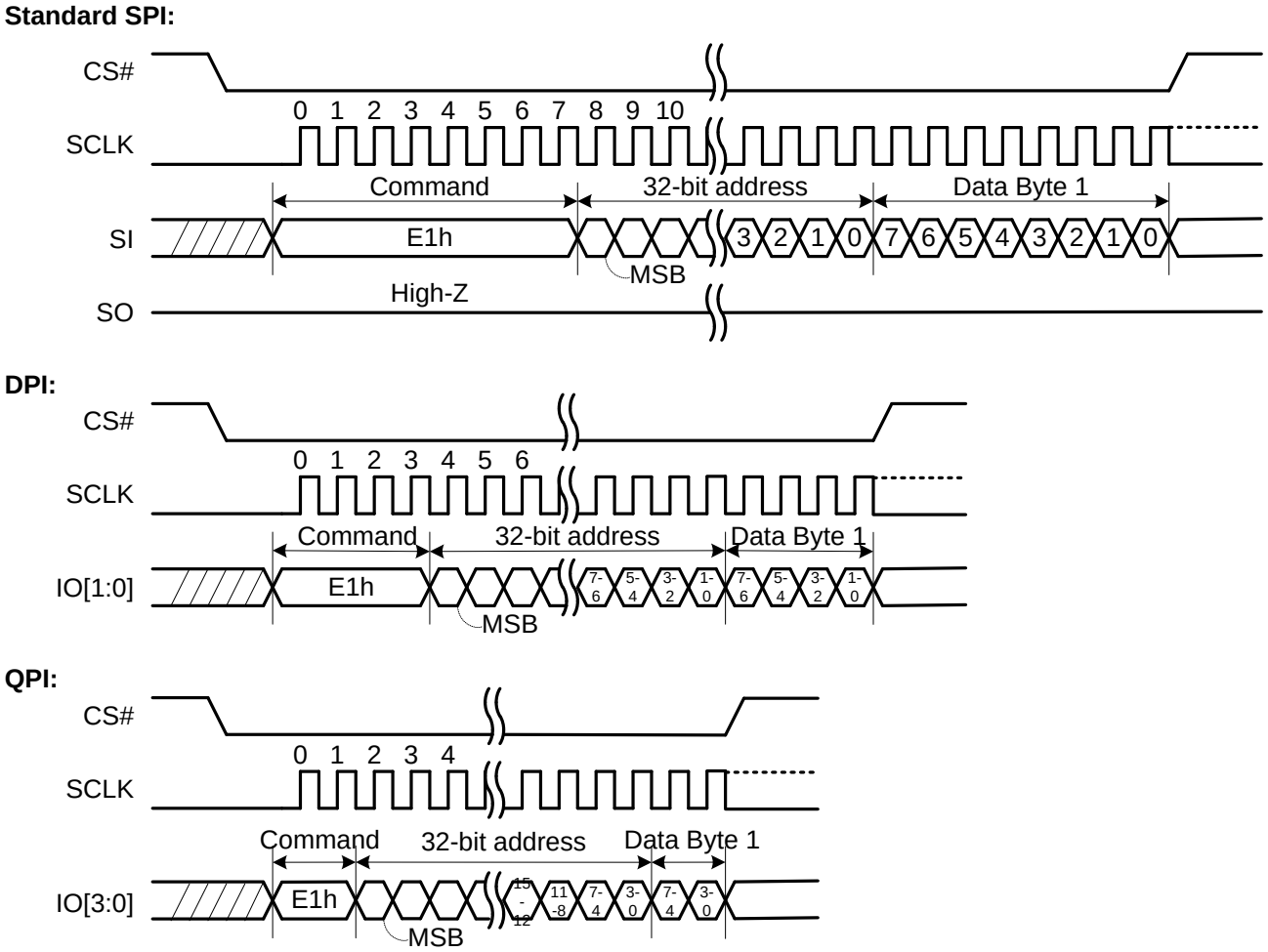


Figure 59: **4-Byte Write Volatile Lock Bits (E1h) Command Sequence**

11. Power Considerations

11.1. Data Protection During Power Transitions

To ensure proper operation, CS# should follow V_{CC} voltage until V_{CC} reaches $V_{CC,min}$ at power-up or V_{SS} at power-down, deselecting the device during power transitions.

While the device is powered up, an internal power-on reset circuitry holds internal logic at reset state, thus protecting the device from inadvertent data modifications. The device does not respond to any incoming commands until V_{CC} reaches a certain threshold voltage, and the host may check the status of the device using the Read Status Register and Read Flag Status Register commands.

Powering down the device during Write, Program or Erase operations may lead to data corruption.

11.2. V_{CC} Decoupling

In hardware design, a decoupling capacitor of 100nF typical should be placed next to V_{CC} pins to stabilize the power supply.

11.3. Power-Up State

After power-up, the device is in the following state:

Device is in standby mode;

WEL bit is reset;

WIP bit is reset;

Dynamic Protection Register is reset.

11.4. Active, Standby and Deep Power-Down

Depending on its power consumption, the device has three power modes.

Table 32: **Power Modes**

Power Mode	Description	Current Consumption
Active Power Mode	When CS# is Low, or when CS# is High but there is ongoing internal operations.	—
Standby Power Mode	When CS# is High and there is no internal operations.	I_{CC1}
Deep Power-Down Mode	Lowest power consumption mode of the device.	I_{CC2}

11.5. Power Loss and Interface Rescue

The device may power up into an unknown state if a Write Nonvolatile Configuration Register command experiences a power loss. In order to place the device back to a known default state (standard SPI without XIP), a Power Loss Recovery Sequence should be used.

If the host and device are out of synchronization, an Interface Rescue Sequence can be used to reset the device interface to a reset state as is defined by the latest nonvolatile configuration register, which only resets the interface instead of the entire device and has no impact on any ongoing operation.

Each of the two sequences consists of two steps, as is shown below, and the order of the two steps must be strictly followed:

Power Loss Recovery Sequence = "Recovery" + "Power Loss Recovery".

Interface Rescue Sequence = "Recovery" + "Interface Rescue".

The above steps are each detailed in a section below. Within each sequence, the tSHSL2 should be at least 50ns.

After a Power Loss Recovery Sequence or Interface Rescue Sequence, a Write nonvolatile Configuration Register command should be used to resolve the issue.

11.5.1. Recovery

Set IO0 and IO3 to 1 and run through the following sequence:

7 SCLK cycles within CS# being Low (CS# toggles High before the 8th SCLK cycle)

+ 9 SCLK cycles within CS# being Low (CS# toggles High before the 10th SCLK cycle)

+ 13 SCLK cycles within CS# being Low (CS# toggles High before the 14th SCLK cycle)

+ 17 SCLK cycles within CS# being Low (CS# toggles High before the 18th SCLK cycle)

+ 25 SCLK cycles within CS# being Low (CS# toggles High before the 26th SCLK cycle)

+ 33 SCLK cycles within CS# being Low (CS# toggles High before the 34th SCLK cycle)

11.5.2. Power Loss Recovery

Set IO0 and IO3 to 1 and run through the following sequence:

8 SCLK cycles within CS# being Low (CS# toggles High before the 9th SCLK cycle)

11.5.3. Interface Rescue

Set IO0 and IO3 to 1 and run through the following sequence:

16 SCLK cycles within CS# being Low (CS# toggles High before the 17th SCLK cycle)

For DTR protocol, the pins should be asserted to 1 for both rising and falling edges of 16 cycles of SCLK.

12. Electrical Characteristics

12.1. Power-On Timing

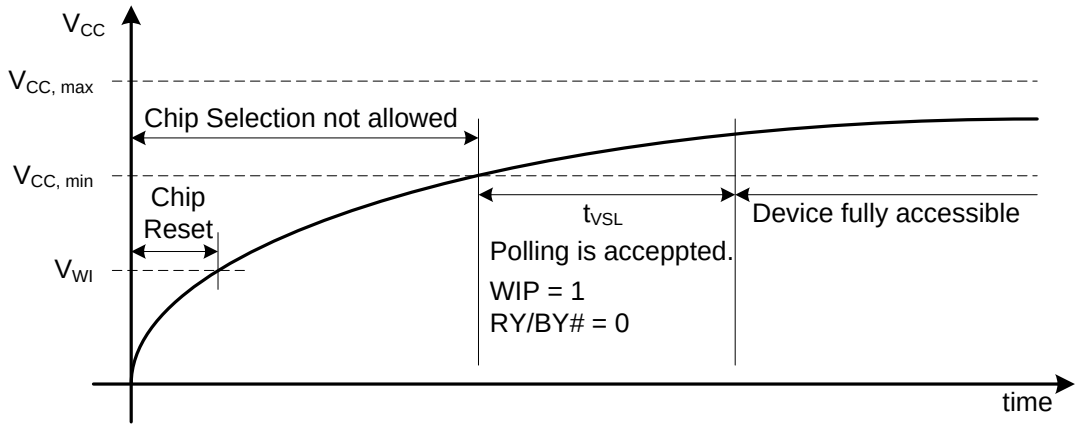


Figure 60: **Power-On Timing Diagram**

Notes:

1. During tVSL, only standard SPI protocol in STR mode supports register polling.
2. During tVSL, HOLD# pin is enabled, RESET# pin is disabled, and IO output drive strength is in its default value.
3. If V_{CC} ramps up very quickly, then after V_{CC} reaches V_{WI} a minimum duration of 100μs is required before polling is accepted.

Table 33: **Power-On Timing and Write Inhibit Threshold**

Symbol	Comments	Typ	Max	Unit
t_{VSL}	$V_{CC, min}$ to earliest CS# Low	—	300	μs
V_{WI}	Write Inhibit Voltage	1.0	1.5	V

12.2. Initial Delivery State

The device is delivered in the following status:

(1) The main memory array is erased; all bits are set to 1 (all bytes are FFh).

(2) The Status Register bits are all set to 0.

(3) Nonvolatile configuration register (NVCR) bits are all set to 1 (FFFFh).

12.3. Absolute Maximum Ratings

Table 34: **Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Unit	Notes
T_{STG}	Storage Temperature	-65	150	℃	
T_{LEAD}	Lead temperature during soldering	—	Note 1	℃	
V_{CC}	Supply Voltage	-0.6	2.4	V	2
V_{IO}	Applied Input / Output Voltage	-0.6	V_{CC}+0.6	V	2
V_{ESD}	ESD Voltage (Human body model)	-2000	2000	V	2, 3

Notes:

1. Compatible with JEDEC Standard J-STD-020C, RoHS, and European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

2. Voltages in this table are with respect to V_{SS} gound.
   Acceptable overshoot range is -0.2V (for less than 20ns), $V_{CC,\,max}$ + 2.0V (for less than 20ns).
3. JEDEC Standard JESD22-A114A.

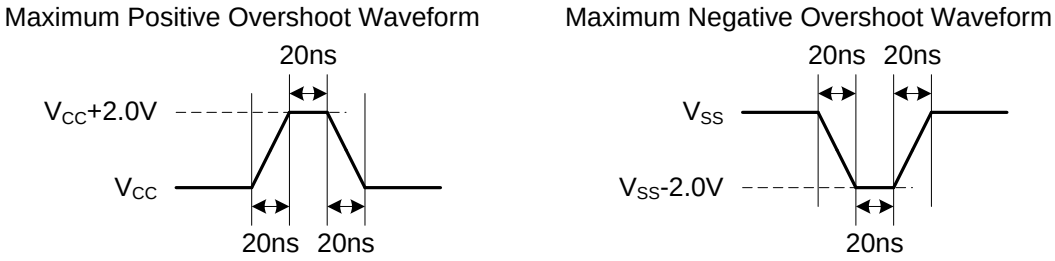


Figure 61: **Maximum Positive / Negative Overshoot Timing Diagram**

12.4. Operating Conditions

Table 35: **Operating Conditions**

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	1.7	2.0	V
T_A	Ambient operating temperature (IT range)	-40	85	℃
T_A	Ambient operating temperature (AT range)	-40	105	℃
T_A	Ambient operating temperature (UT range)	-40	125	℃

12.5. Input/Output Capacitance

Table 36: **Input/Output Capacitance**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$C_{IN/OUT}$	Input/Output capacitance for IO0 through IO3	V_{OUT}=0V	—	—	10	pF
C_{IN}	Input capacitance (other pins)	V_{IN}=0V	—	—	6	pF
$C_{IN/CS\#}$	Input capacitance (CS# pin)	V_{IN}=0V	—	—	10	pF

Notes:

1. These parameters are not 100% tested.
2. These parameters are tested at T_A=25℃ and SCLK frequency = 54MHz.

12.6. AC Timing Input/Output Conditions

Table 37: **Capacitance Measurement Conditions**

Symbol	Parameter	Min	Typ	Max	Unit	Note
C_L	Load Capacitance	—	—	30	pF	1
—	Input Rise And Fall time	—	—	1.5	ns	
	Input Pulse Voltage	0.2V_{CC} to 0.8V_{CC}			V	2
	Input Timing Reference Voltage	0.3V_{CC} to 0.7V_{CC}			V	
	Output Timing Reference Voltage	0.5V_{CC}			V	

Notes:

1. Output drive strength is user configurable.
2. For DPI and QPI operations: 0V to V_{CC}.

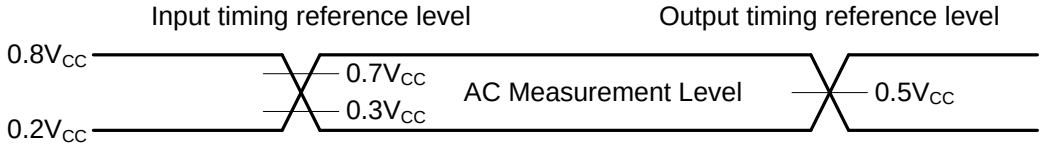


Figure 62: **Input Test Waveform and Measurement Level**

12.7. DC Characteristics

12.7.1. DC Current Characteristics

Table 38: **DC Current Characteristics and Operating Conditions**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	—	—	—	±2	μA
I_{LO}	Output Leakage Current	—	—	—	±2	μA
I_{CC1}	Standby Current	CS#=V_{CC}, V_{IN}=V_{CC} or V_{SS}	—	20	100	μA
I_{CC2}	Deep Power-Down Current	CS#=V_{CC}, V_{IN}=V_{CC} or V_{SS}	—	2	50	μA
I_{CC3}	Operating Current (Read)	CLK=0.1V_{CC} / 0.9V_{CC} at 120MHz, Q=Open(*1,*2,*4 I/O)	—	15	20	mA
		CLK=0.1V_{CC} / 0.9V_{CC} at 80MHz, Q=Open(*1,*2,*4 I/O)	—	13	18	mA
I_{CC4}	Operating Current (PP)	CS#=V_{CC}	—	—	20	mA
I_{CC5}	Operating Current(WRSR)	CS#=V_{CC}	—	—	20	mA
I_{CC6}	Operating Current (SE)	CS#=V_{CC}	—	—	20	mA

Notes:

1. All current values are RMS unless otherwise noted.
2. Standby current is the average value over any duration of 5μs after CS# is deasserted and the device is idle.
3. Deep power-down current is the average value over any duration of 5ms after the device has been in Deep Power-Down mode for at least 100μs.
4. Read currents are the average value of any 1K-byte continuous read using check-board data pattern with no load.
5. Program currents are the average value of any 256-byte program of typical data.

12.7.2. DC Voltage Characteristics

Table 39: **DC Voltage Characteristics and Operating Conditions**

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	—	—	—	0.2V_{CC}	V
V_{IH}	Input High Voltage	—	0.7V_{CC}	—	—	V
V_{OL}	Output Low Voltage	I_{OL} =100μA	—	—	0.2	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	V_{CC}-0.2	—	—	V

Notes:

1. V_{IL} can undershoot to -1.0V (for a duration of less than 2ns), and V_{IH} can overshoot to $V_{CC,max}$+1.0V(for a duration of less than 2ns).

12.8. AC Characteristics

12.8.1. Maximum Clock Frequency

Table 40: **Maximum Clock Frequency**

Symbol	Parameter	Single IO	Single IO	Dual IO	Dual IO	Quad IO	Quad Io

		STR	DTR	STR	DTR	STR	DTR
fC	Clock frequency for all commands except Read.	166	90	166	90	166	90
fR	Clock frequency for 03h Read commands.	54	27	—	—	—	—

Notes:

1. Frequency unit is MHz.

12.8.2. AC Characteristics

Table 41: **AC Characteristics**

Symbol	Parameter	Protocol	Min	Typ	Max	Unit	Note
t_{CH}	Serial Clock High Time	STR	3.5	—	—	ns	2, 3
t_{CH}	Serial Clock High Time	DTR					2, 3
t_{CL}	Serial Clock Low Time	STR	3.5	—	—	ns	2, 4
t_{CL}	Serial Clock Low Time	DTR					2, 4
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	STR/DTR	0.1	—	—	V/ns	5, 6
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	STR/DTR	0.1	—	—	V/ns	5, 6
t_{SLCH}	CS# Active Setup Time	STR/DTR	5	—	—	ns	
t_{CHSL}	CS# Not Active Hold Time	STR/DTR	5	—	—	ns	
t_{DVCH}	Data In Setup Time	STR/DTR	2	—	—	ns	
t_{DVCL}	Data In Setup Time	DTR only					
t_{CHDX}	Data In Hold Time	STR	2	—	—	ns	
t_{CHDX}	Data In Hold time	DTR					
t_{CLDX}	Data In Hold Time	DTR only					
t_{CHSH}	CS# Active Hold Time (relative to SCLK)	STR	5	—	—	ns	
t_{CHSH}	CS# Active Hold Time (relative to SCLK)	DTR					
t_{CLSH}	CS# Active hold time (relative to SCLK Low) Only for DTR writes	DTR only					
t_{SHCH}	CS# Not Active Setup Time (relative to SCLK)	STR	5	—	—	ns	
t_{SHCH}	CS# Not Active Setup Time (relative to SCLK)	DTR					
t_{SHSL1}	CS# High Time (After a Read command)	STR/DTR	20	—	—	ns	
t_{SHSL2}	CS# High Time (After a non-Read comand)	STR/DTR					7
t_{SHQZ}	Output Disable Time	STR/DTR	—	—	6	ns	5
t_{CLQV}	Clock Low To Output Valid at 30pF	STR/DTR	—	—	7	ns	
t_{CLQV}	Clock Low To Output Valid at 10pF	STR/DTR					
t_{CHQV}	Clock High To Output Valid at 30pF	DTR only	—	—	7	ns	
t_{CHQV}	Clock High To Output Valid at 10pF	DTR only					
t_{CLQX}	Output Hold Time	STR/DTR	1.2	—	—	ns	
t_{CHQX}	Output Hold Time	DTR only	1.2	—	—	ns	
t_{HLCH}	HOLD# Low Setup Time (relative to Clock)	STR/DTR	5	—	—	ns	
t_{CHHH}	HOLD# Low Hold Time (relative to Clock)	STR/DTR	5	—	—	ns	
t_{HHCH}	HOLD# High Setup Time (relative to Clock)	STR/DTR	5	—	—	ns	
t_{CHHL}	HOLD# High Hold Time (relative to Clock)	STR/DTR	5	—	—	ns	
t_{HHQX}	HOLD# High To Low-Z Output	STR/DTR	—	—	6	ns	5

t_{HLQZ}	HOLD# Low To High-Z Output	STR/DTR	—	—	6	ns	5
t_{WHSL}	Write Protect Setup Time Before CS# Low	STR/DTR	20	—	—	ns	8
t_{SHWL}	Write Protect Hold Time After CS# High	STR/DTR	100	—	—	ns	8
t_{DP}	CS# High To Deep Power-Down Mode	STR/DTR	—	—	20	μs	
t_{RDP}	CS# High To Standby Mode (DPD exit time)	STR/DTR	—	—	20	μs	
t_W	Write Status Register Cycle Time	STR/DTR	—	5	30	ms	
t_{WNVCR}	Write Nonvolatile Configuration Register Cycle time	STR/DTR					
t_{PPBP}	Nonvolatile sector lock time	STR/DTR					
t_{ASPP}	Program ASP register	STR/DTR					
t_{PASSP}	Program Password	STR/DTR					
t_{PPBE}	Erase nonvolatile sector lock array	STR/DTR					
t_{PP}	Page Programming Time (256 bytes)	STR/DTR	—	0.6	2.4	ms	9
t_{PP}	Page Program Time (n bytes)	STR/DTR					10
t_{POTP}	Program OTP cycle time	STR/DTR					
t_{SE}	Sector Erase Time(4K Bytes)	STR/DTR	—	50	200/300(2)	ms	
t_{BE1}	Block Erase Time(32K Bytes)	STR/DTR	—	0.15	0.8/1.6(3)	s	
t_{BE2}	Block Erase Time(64K Bytes)	STR/DTR	—	0.20	1.2/2.0(4)	s	
t_{CE}	Chip Erase Time(NM25LQ512A)	STR/DTR	—	25	60	s	

Notes:

1. This table gives typical values at T_A=25℃.
2. tCH+tCL should equal to 1/fC.
3. Only for AT parts in QPI: tCH in STR is 3.375ns min, tCH in DTR is 5.62ns min.
4. Only for AT parts in QPI: tCH in STR is 3.375ns min, tCH in DTR is 5.62ns min.
5. Value is not 100% tested and is guaranteed by characterization.
6. Expressed in terms of slew rate.
7. Non-Read commands include: Write, Program, Erase.
8. Applicable only for Write Status Register command when Status Register Write is 1.
9. This value is for typical data pattern with 50% "0" and 50% "1".
10. The symbol "int(n)" is the integer part of n.

12.8.3. AC Reset Characteristics

Table 42: **AC Reset Characteristics**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tRLRH	Reset pulse width	—	3.5	—	—	ns
tRHSL	Reset recovery time	CS# is High, XIP mode.				ns
		CS# is High, Standby mode.	3.5	—	—	ns
		Command decode in progress, Read operation in progress or Write operation to volatile registers in progress.				ns
		Array Program/Erase/Suspend/Resume, Program OTP, Nonvolatile Sector Lock, or Erase Nonvolatile Sector Lock Array	0.1	—	—	μs

		command in progress.				
		Write Status Register operation in progress				ms
		Write Nonvolatile Configuration Register operation in progress				ms
		Sector or Block Erase operation complete or in suspension.				s
		Deep power-down mode.				ms
		Advanced Sector Protection Program operation in progress.				ms
		Password Protection Program in progress				ms
tSHSL3	Software reset recovery time	CS# is High, Standby Mode.				ns
		Array Program/Erase/Suspend/Resume, Program OTP, Nonvolatile Sector Lock, or Erase Nonvolatile Sector Lock Array command in progress.				μs
		Write Status Register operation in progress	0.1	—	—	ms
		Write Nonvolatile Configuration Register operation in progress				ms
		Sector or Block Erase operation complete or in suspension.				s
		Deep power-down mode.				ms
		Advanced Sector Protection Program operation in progress.				ms
		Password Protection Program in progress				ms

Notes:

1. Values in this table are not 100% tested and are guaranteed by characterization.
2. If tRLRH < 50ns, device is not guaranteed to be reset.

12.9. AC Timing Diagrams

12.9.1. Reset AC Timing During Program/Erase Cycles

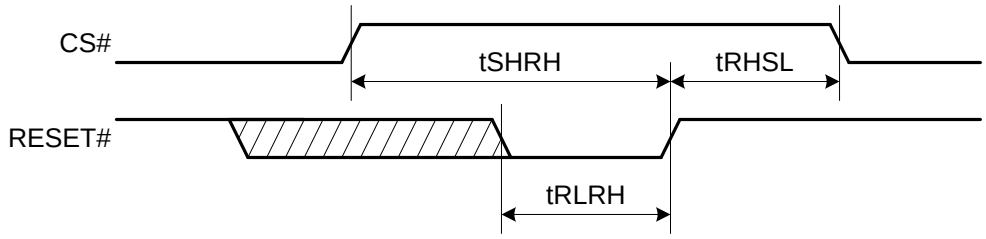


Figure 63: **Reset AC Timing Diagram During Program/Erase Cycles**

12.9.2. Reset Enable and Reset Memory Timing

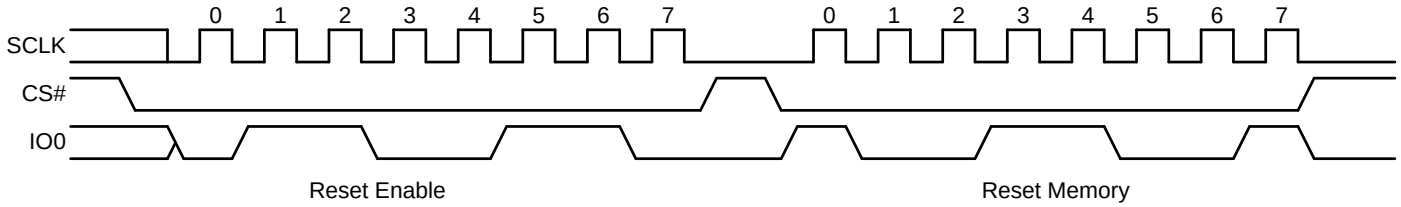


Figure 64: **Reset Enable and Reset Memory Timing**

12.9.3. Serial Input Timing STR

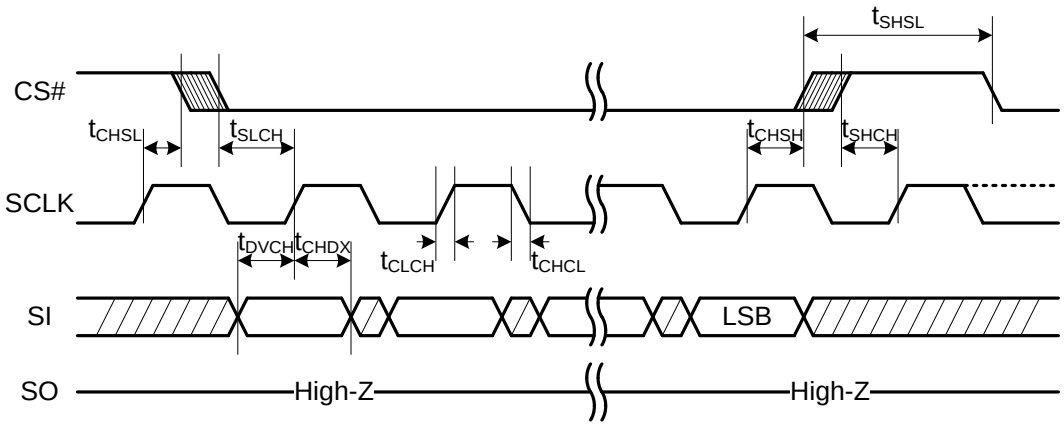


Figure 65: **Serial Input Timing STR**

12.9.4. Serial Input Timing DTR

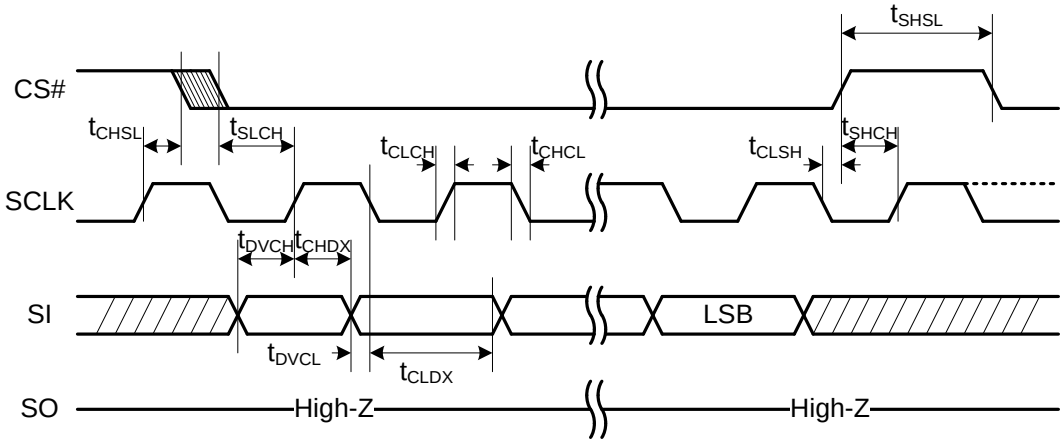


Figure 66: **Serial Input Timing DTR**

12.9.5. Write Protect Setup and Hold During Write Status Register Operation (SRWD=1)

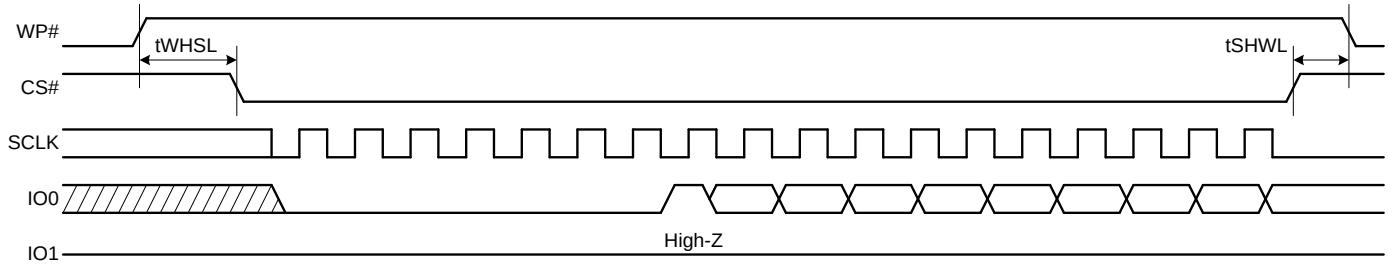


Figure 67: **Write Protect Setup and Hold During Write Status Register Operation (SRWD=1)**

12.9.6. Hold Timing Diagram

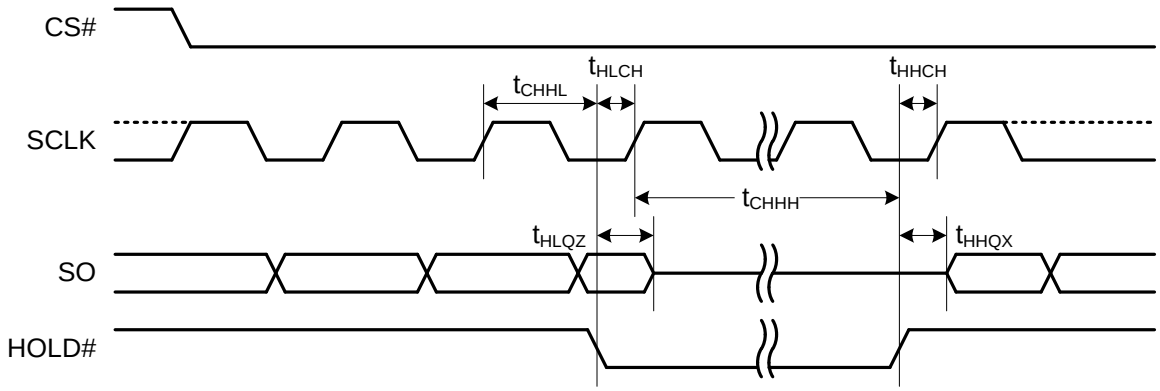


Figure 68: **Hold Timing Diagram**

12.9.7. Serial Output Timing STR

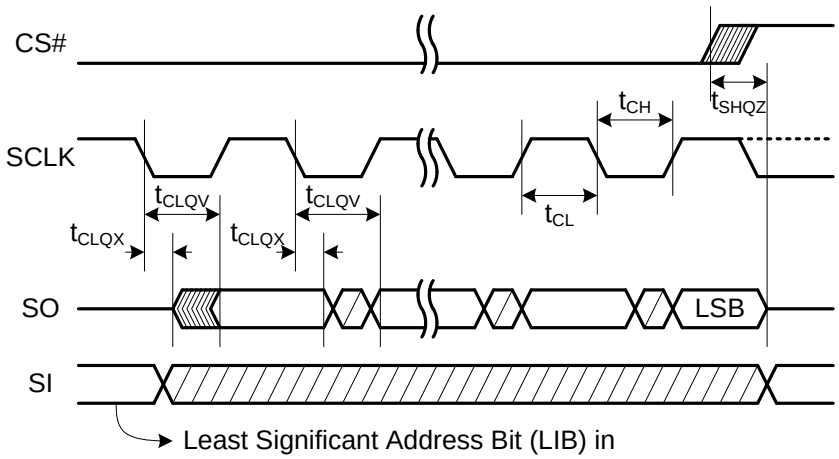


Figure 69: **Serial Output Timing STR**

12.9.8. Serial Output Timing DTR

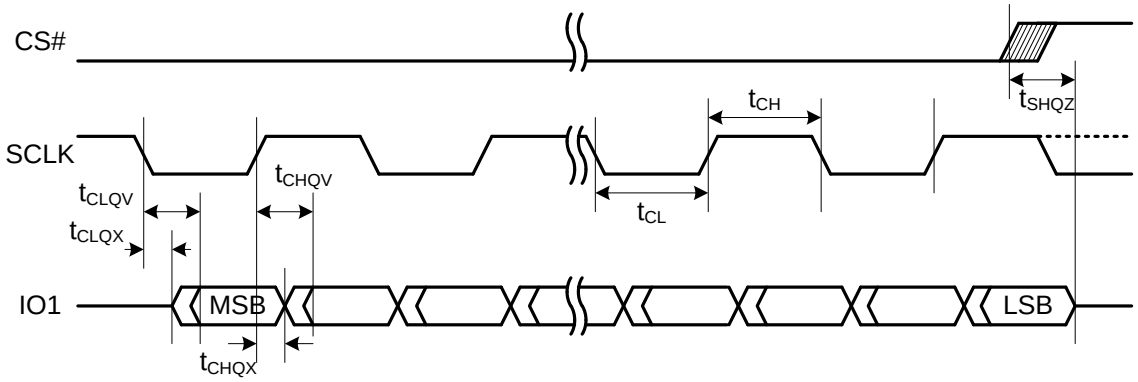


Figure 70: **Serial Output Timing DTR**

12.10.Program and Erase Specifications

Table 43: **Program/Erase Specifications**

Parameter	Condition	Typ	Max	Units	Note
Erase to suspend	Erase resume to erase suspend	150	—	µs	1
Program to suspend	Program resume to program suspend	5	—	µs	1

Sector or Block Erase to suspend	Sector or Block Erase resume to erase suspend	50	—	µs	1
Suspend latency	Program	7	25	µs	2
Suspend latency	Sector or Block erase	15	30	µs	2
Suspend latency	Chip Erase	15	30	µs	3

Notes:

1. The device does internally control the timing.
2. During suspend, any Read command is accepted.
3. During suspend, any command are expected except:
   4KB Sector Erase, 32KB Block Erase, 64KB Block Erase, Chip Erase;
   Write Status Register;
   Write Nonvolatile Configuration Register;
   Program OTP.

12.11.Quality and Reliability Characteristics

Table 44: **Quality and Reliability Characteristics**

Symbol	Description	Min	Typ	Max	Units
T_{DR}	Data retention	—	20	—	Years
N_{PE}	Program/erase cycles (Endurance)	100,000	—	—	Cycles

13. Ordering Information

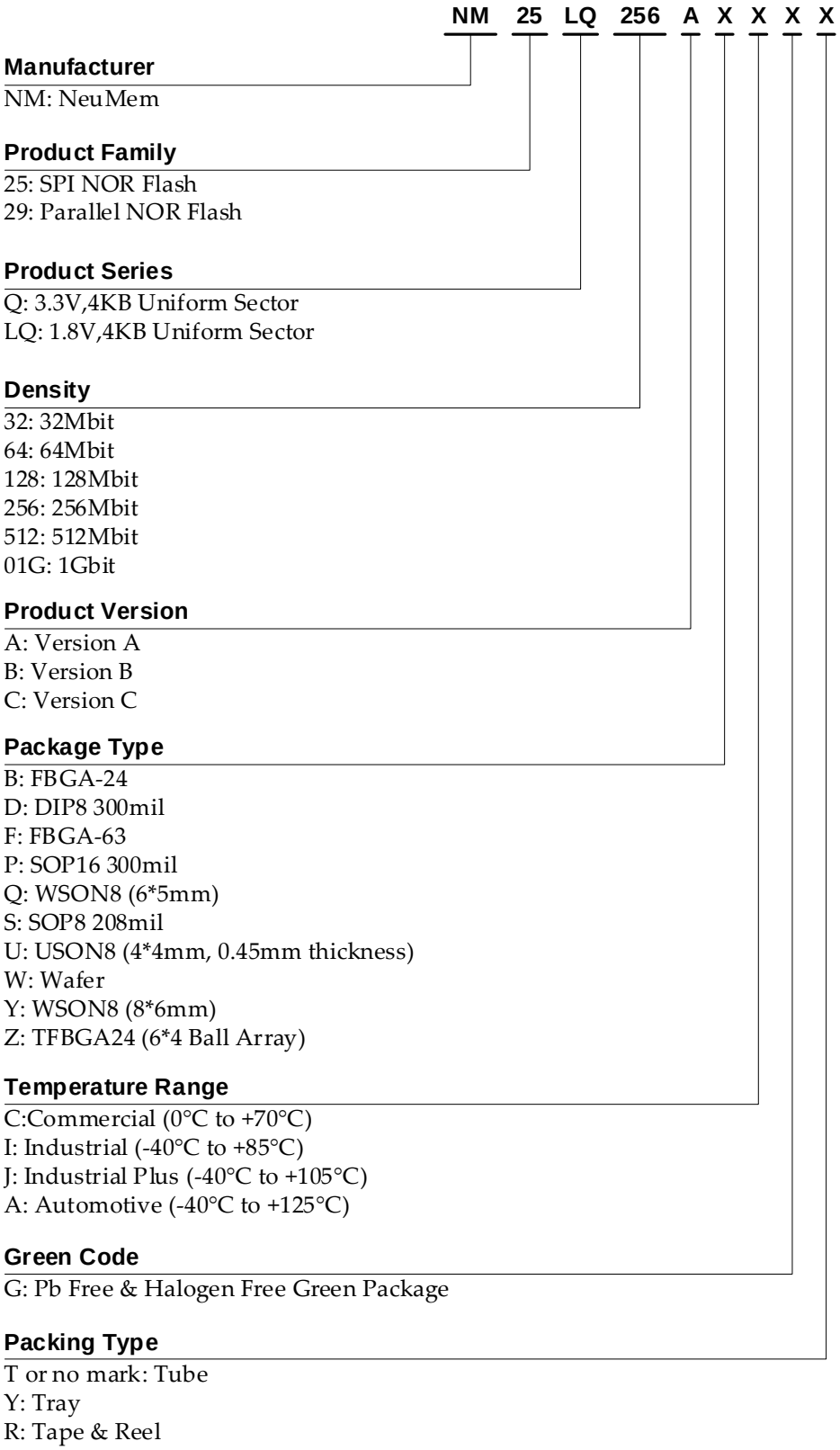


Figure 71: **Device Ordering Information**

14. Package Information

14.1. SOP8 (208mil)

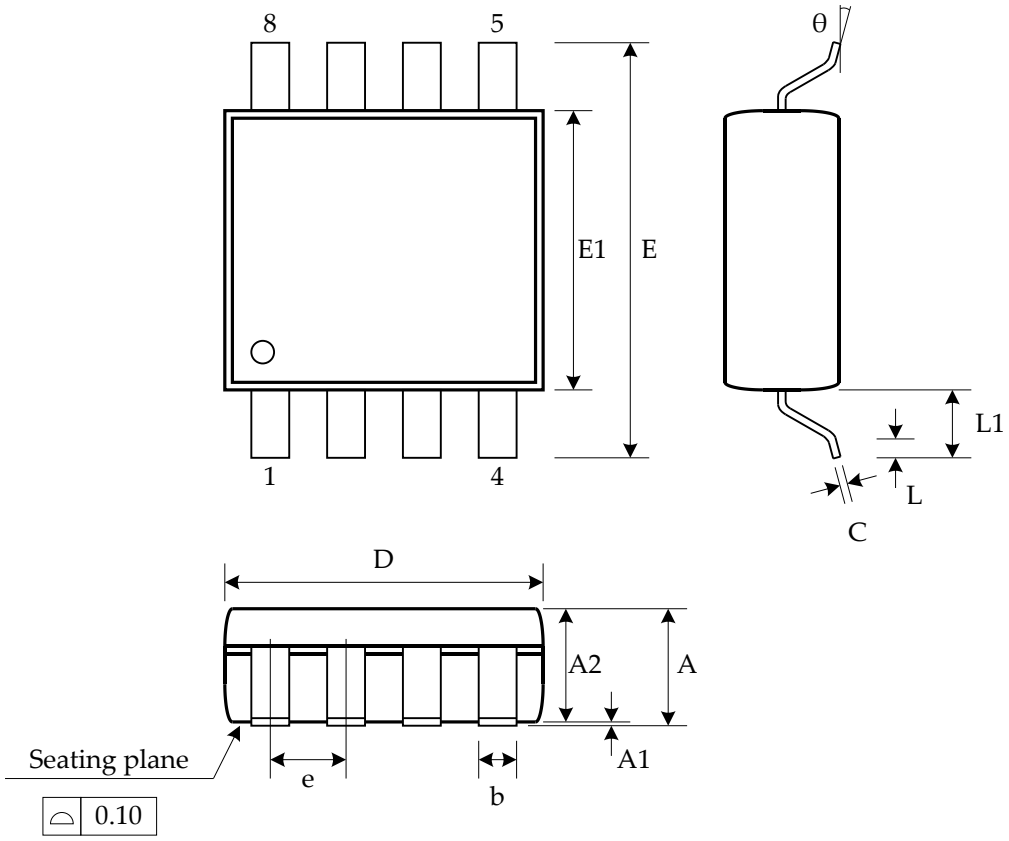


Figure 72: **SOP8(208mil) Package**

Table 45: **The Package Dimensions of SOP8(208mil)**

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
mm	MIN.		0.05	1.70	0.31	0.18	5.13	7.70	5.18		0.50	1.20	0
	NOM.		0.15	1.80	0.41	0.21	5.23	7.90	5.28	1.27 BSC	0.67	1.31	5
	MAX.	2.16	0.25	1.91	0.51	0.25	5.33	8.10	5.38		0.85	1.41	8
Inch	MIN.		0.002	0.067	0.012	0.007	0.202	0.303	0.204		0.020	0.048	0
	NOM.		0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050 BSC	0.026	0.052	5
	MAX.	0.085	0.010	0.075	0.020	0.010	0.210	0.319	0.212		0.033	0.056	8

Notes:

1. Package length and width do not include mold flash.
2. Seating plane: Max. 0.10mm.

14.2. DIP8 (300mil)

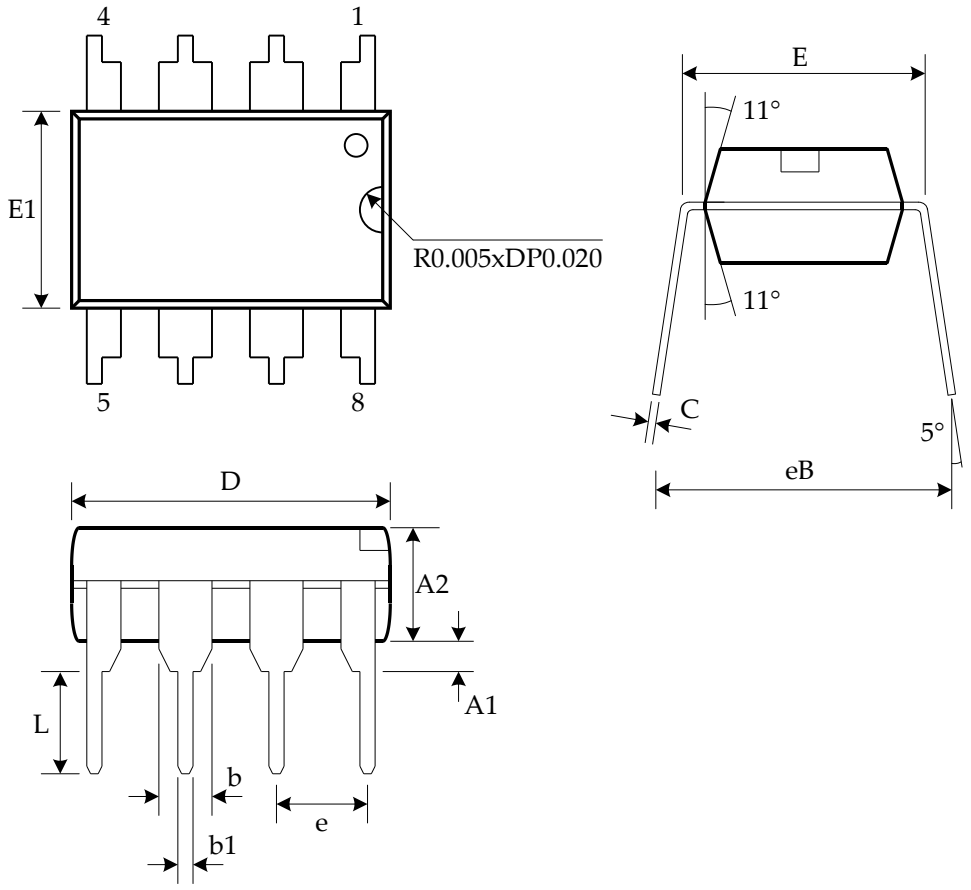


Figure 73: **DIP8(300mil) Package**

Table 46: **The Package Dimensions of DIP8(300mil)**

Symbol / Unit		A1	A2	b	b1	C	D	E	E1	e	eB	L
mm	MIN.	0.38	3.00	1.27	0.38	0.20	9.05	7.62	6.12		7.62	3.04
	NOM.	0.72	3.25	1.46	0.46	0.28	9.32	7.94	6.38	2.54	8.49	3.30
	MAX.	1.05	3.50	1.65	0.54	0.34	9.59	8.26	6.64		9.35	3.56
Inch	MIN.	0.015	0.118	0.050	0.015	0.008	0.356	0.300	0.242		0.333	0.120
	NOM.	0.028	0.128	0.058	0.018	0.011	0.367	0.313	0.252	0.100	0.345	0.130
	MAX.	0.041	0.138	0.065	0.021	0.014	0.378	0.326	0.262		0.357	0.140

Notes:

1. Package length and width do not include mold flash.

14.3. WSON8 (6*5mm)

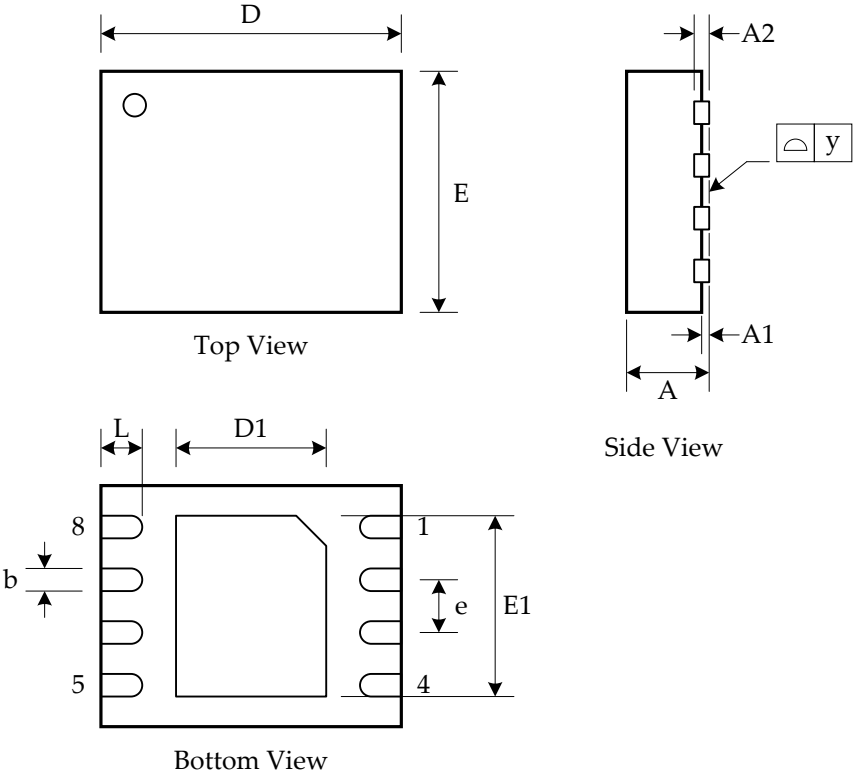


Figure 74: **WSON8(6*5mm) Package**

Table 47: **The Package Dimensions of WSON8(6*5mm)**

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	MIN.	0.70		0.19	0.35	5.90	3.25	4.90	3.85		0.00	0.50
	NOM.	0.75		0.22	0.42	6.00	3.37	5.00	3.97	1.27 BSC	0.04	0.60
	MAX.	0.80	0.05	0.25	0.48	6.10	3.50	5.10	4.10		0.08	0.75
Inch	MIN.	0.028		0.007	0.014	0.232	0.128	0.193	0.151		0.000	0.020
	NOM.	0.030		0.009	0.016	0.236	0.133	0.197	0.156	0.050 BSC	0.001	0.024
	MAX.	0.032	0.002	0.010	0.019	0.240	0.138	0.201	0.161		0.003	0.030

Notes:

1. Package length and width do not include mold flash.
2. The exposed metal pad on the bottom of the package is connected to device ground (GND pin), so that it can either connect to GND or be left floating.

14.4. WSON8 (8*6mm)

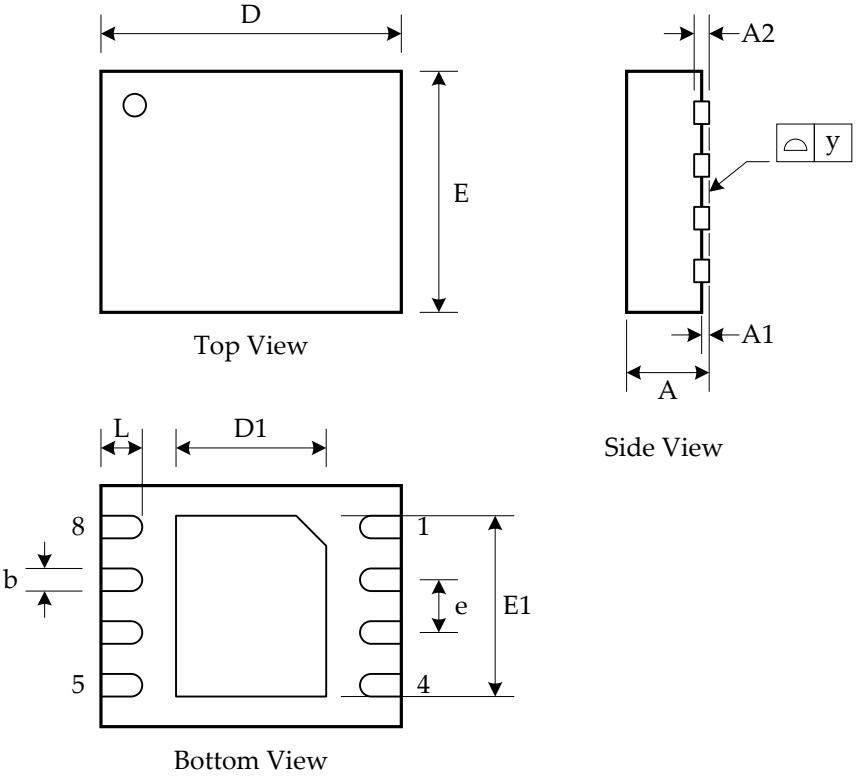


Figure 75: **WSON8(8*6mm) Package**

Table 48: **The Package Dimensions of WSON8(8*6mm)**

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	MIN.	0.70			0.35	7.90	3.25	5.90	4.15		0.00	0.55
	NOM.	0.75		0.20	0.40	8.00	3.42	6.00	4.22	1.27	0.04	0.60
	MAX.	0.80	0.05		0.45	8.10	3.50	6.10	4.40		0.08	0.65
Inch	MIN.	0.028			0.014	0.311	0.128	0.232	0.163		0.000	0.022
	NOM.	0.030		0.008	0.016	0.315	0.135	0.236	0.166	0.050	0.001	0.024
	MAX.	0.032	0.002		0.019	0.319	0.138	0.240	0.173		0.003	0.027

Notes:

1. Package length and width do not include mold flash.
2. The exposed metal pad on the bottom of the package is connected to device ground (GND pin), so that it can either connect to GND or be left floating.

14.5. TFBGA-24(6*4 ball array)

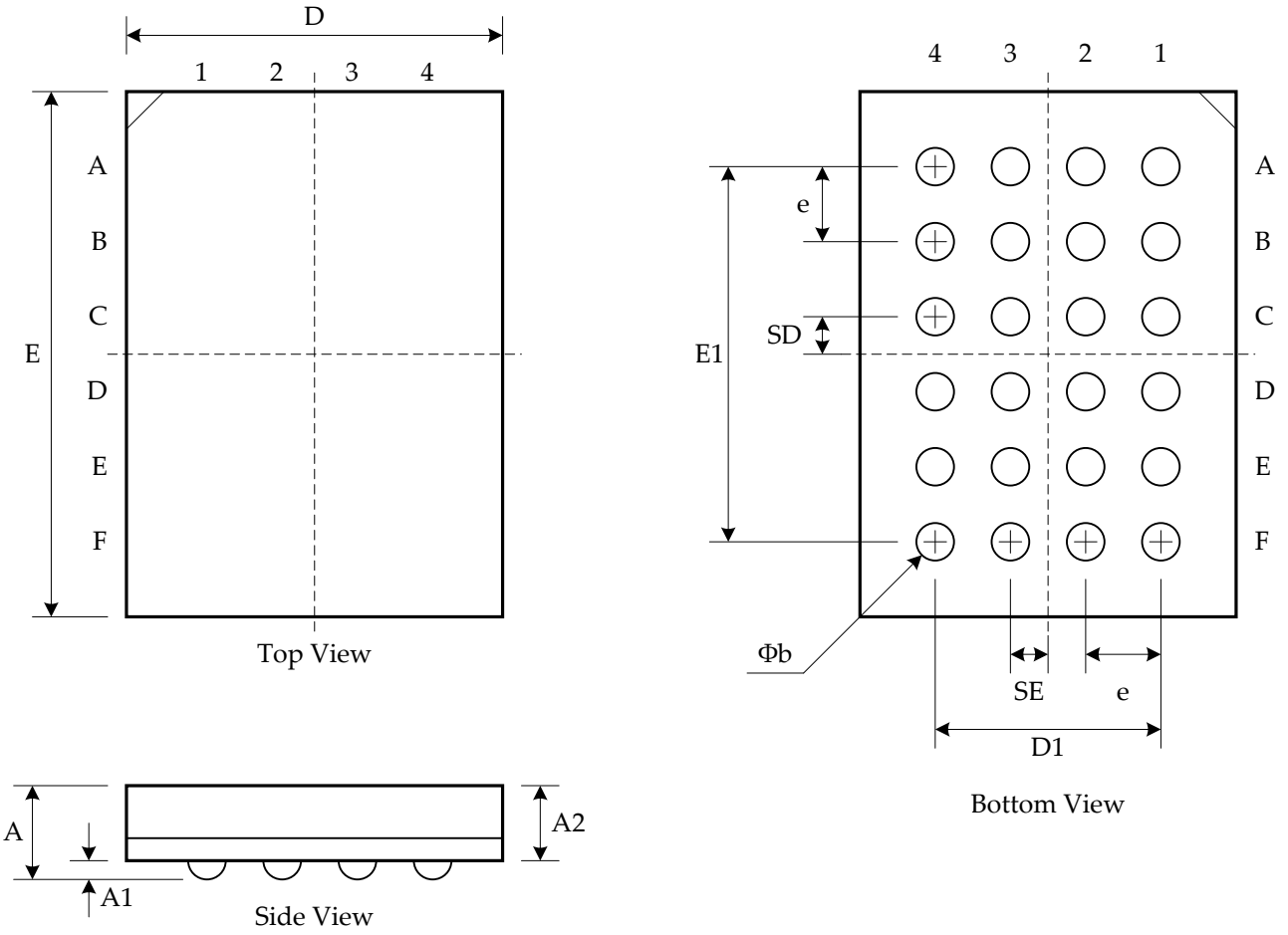


Figure 76: **TFBGA-24(6*4 ball array) Package**

Table 49: **The Package Dimensions of TFBGA-24(6*4 ball array)**

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	SE	SD
mm	MIN.		0.25		0.35	5.95	3.00 BSC	7.95	5.00 BSC	1.00 BSC	0.50 TYP	0.50 TYP
	NOM.		0.30	0.85	0.40	6.00		8.00				
	MAX.	1.20	0.35		0.45	6.05		8.05				
Inch	MIN.		0.010		0.014	0.234	0.118 BSC	0.313	0.197 BSC	0.039 BSC	0.020 TYP	0.020 TYP
	NOM.		0.012	0.033	0.016	0.236		0.315				
	MAX.	0.047	0.014		0.018	0.238		0.317				

Notes:

1. Package length and width do not include mold flash.

14.6. SOP16 (300mil)

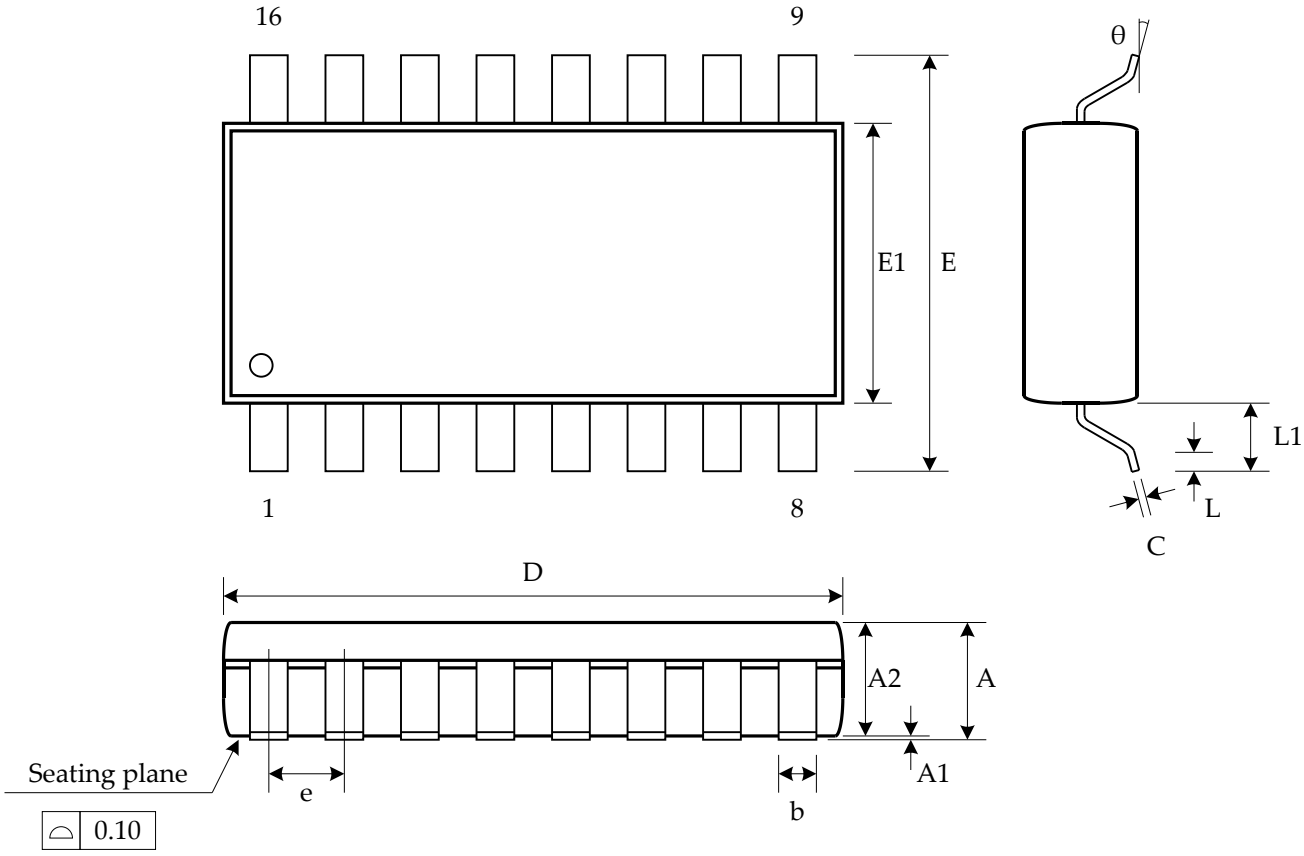


Figure 77: **SOP16(300mil) Package**

Table 50: **The Package Dimensions of SOP16(300mil)**

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
mm	MIN.	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0
	NOM.	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27 BSC	0.84	1.44	5
	MAX.	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	8
Inch	MIN.	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0
	NOM.	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050 BSC	0.033	0.057	5
	MAX.	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	8

Notes:

1. Package length and width do not include mold flash.
2. Seating plane: Max. 0.10mm.

14.7. USON8 (4*4mm)

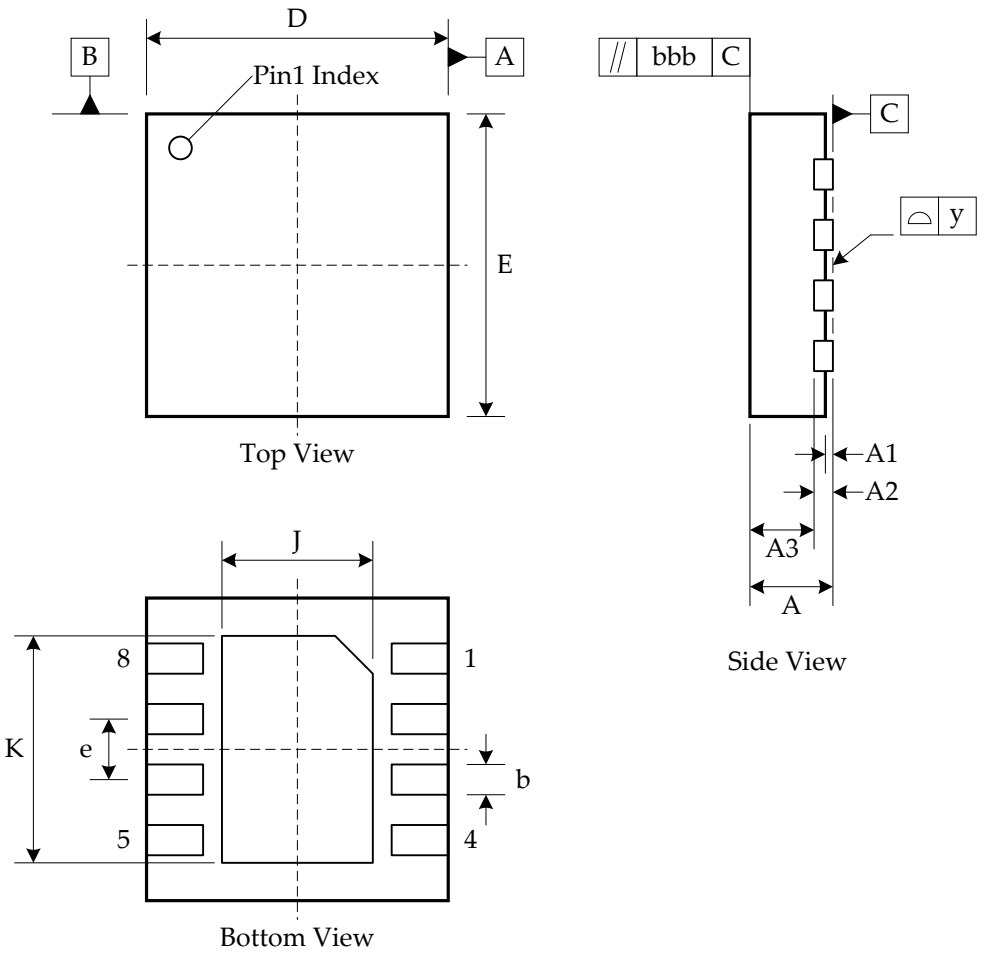


Figure 78: **USON8(4*4mm) Package**

Table 51: **The Package Dimensions of USON8(4*4mm)**

Symbol / Unit		A	A1	A2	A3	b	D	E	e	J	K	L
mm	MIN.	0.40	0.00	0.15 REF	0.25	0.25	3.90	3.90	0.8 BSC	2.20	2.90	0.35
	NOM.	0.45	---		0.30	0.30	4.00	4.00		2.30	3.00	0.40
	MAX.	0.50	0.05		0.35	0.35	4.10	4.10		2.40	3.10	0.45
Inch	MIN.	0.015	0.000	0.15 REF	0.009	0.009	0.153	0.153	0.8 BSC	0.086	0.114	0.013
	NOM.	0.017	---		0.011	0.011	0.157	0.157		0.090	0.118	0.015
	MAX.	0.019	0.001		0.013	0.013	0.161	0.161		0.094	0.122	0.017

Notes:

1. Package length and width do not include mold flash.
2. The exposed metal pad on the bottom of the package is connected to device ground (GND pin), so that it can either connect to GND or be left floating.

14.8. SOP8 (150mil)

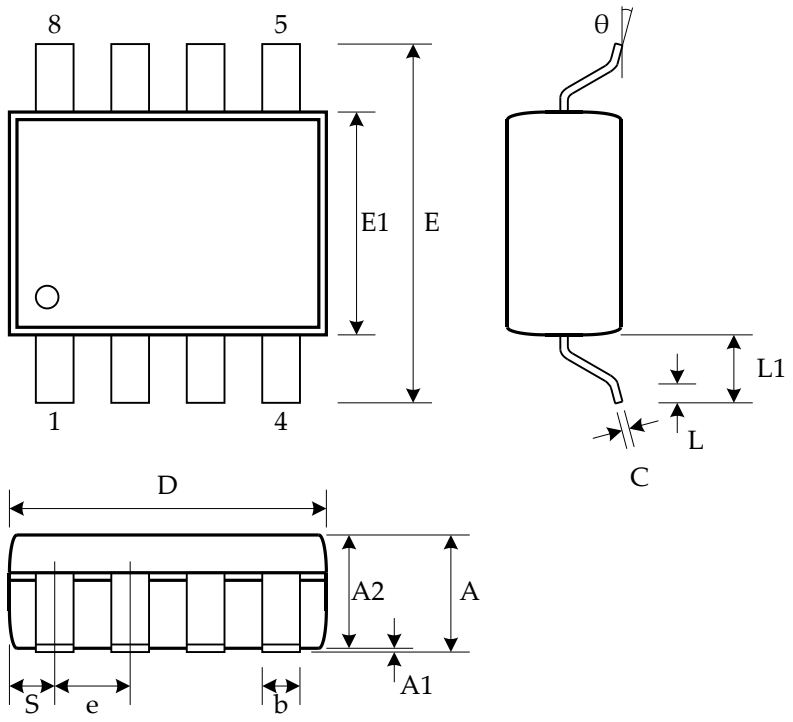


Figure 79: **SOP8(150mil) Package**

Table 52: **The Package Dimensions of SOP8(150mil)**

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	MIN.	--	0.10	1.35	0.36	0.15	4.77	5.80	3.80	--	0.46	0.85	0.41	0
	NOM.	--	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5
	MAX.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00	--	0.86	1.25	0.67	8
Inch	MIN.	--	0.004	0.053	0.014	0.006	0.188	0.228	0.150	--	0.018	0.033	0.016	0
	NOM.	--	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.05	0.026	0.041	0.021	5
	MAX.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158	--	0.034	0.049	0.026	8

Notes:

1. Package length and width do not include mold flash.

14.9. USON8 (4*3mm)

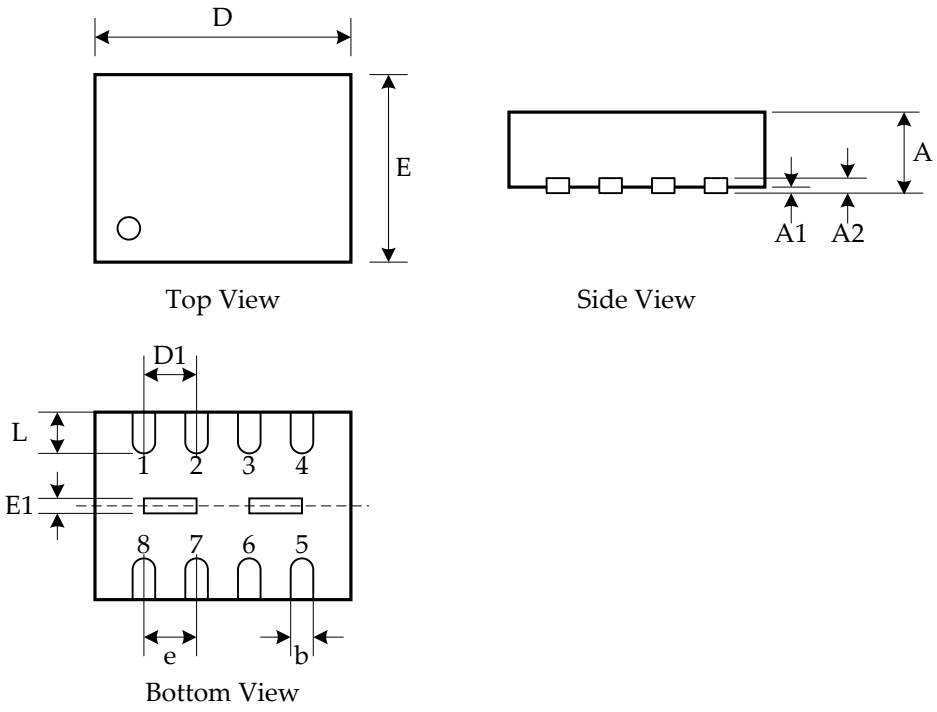


Figure 80: **USON8(4*3mm) Package**

Table 53: **The Package Dimensions of USON8(4*3mm)**

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	L
mm	MIN.	0.50	0.00	00	0.25	3.90	0.70	2.90	0.10	0.80 BSC	0.55
	NOM.	0.55	0.02	0.15	0.30	4.00	0.80	3.00	0.20		0.60
	MAX.	0.60	0.05	00	0.35	4.10	0.90	3.10	0.30		0.65
Inch	MIN.	0.020	0.000	00	0.010	0.153	0.027	0.114	0.004	0.31 BSC	0.022
	NOM.	0.022	0.001	0.006	0.012	0.157	0.031	0.118	0.008		0.024
	MAX.	0.024	0.002	00	0.014	0.161	0.035	0.122	0.012		0.026

Notes:

1. Package length and width do not include mold flash.
2. The exposed metal pad on the bottom of the package is connected to device ground (GND pin), so that it can either connect to GND or be left floating.

15. Revision History

The table below shows the revision history of this document.

Date	Version	Revision
Jan 17, 2021	v1.0	NeuMem initial release.

16. Important Notice

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